Freescale Semiconductor
Data Sheet: Advance Information

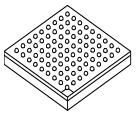
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RoHS

MCIMX53xA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

i.MX53xA Automotive and Infotainment Applications Processors



Package Information
Plastic Package
Case TEPBGA-2 19 x 19 mm, 0.8 mm pitch

Ordering Information
See Table 1 on page 3

1 Introduction

The MCIMX53xA (i.MX53xA) automotive infotainment processor is Freescale Semiconductor's latest addition to a growing family of multimedia-focused products offering high performance processing with a high degree of functional integration aimed at the growing automotive infotainment, telematics, HMI, and display-based cluster markets. This device includes 3D and 2D graphics processors, 1080i/p video processing, and dual display, and provides a variety of interfaces.

The i.MX53xA processor features Freescale's advanced implementation of the ARM™ core, which operates at clock speeds as high as 800 MHz and interfaces with DDR2/LVDDR2-800, LPDDR2-800, or DDR3-800 DRAM memories. This device is well-suited for graphics rendering for HMI and navigation, high performance speech processing with large databases, video processing and display, audio playback, and many other applications.

The flexibility of the i.MX53xA architecture allows for its use in a wide variety of applications. As the heart of the application chipset, the i.MX53xA processor

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ARM POWERED

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provides all the interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, camera sensors, and dual displays.

Features of the i.MX53xA processor include the following:

- Multilevel memory system—The multilevel memory system of the i.MX53xA is based on the L1 instruction and data caches, L2 cache, internal and external memory. The i.MX53xA supports many types of external memory devices, including DDR2, low voltage DDR2, LPDDR2, DDR3, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND including eMMC up to rev 4.4.
- Smart speed technology—The i.MX53xA device has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart Speed Technology enables the designer to deliver a feature-rich product requiring levels of power far lower than industry expectations.
- Multimedia powerhouse—The multimedia performance of the i.MX53xA processor ARM core is boosted by a multilevel cache system, Neon (including advanced SIMD, 32-bit single-precision floating point support) and vector floating point coprocessors. The system is further enhanced by a multistandard hardware video codec, autonomous image processing unit (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration— The i.MX53xA processors provide two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator (33 Mtri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance) and an OpenVG™ 1.1 2D graphics accelerator (200 Mpix/s).
- Interface flexibility—The i.MX53xA processor supports connection to a variety of interfaces, including LCD controller for two displays and CMOS sensor interface, high-speed USB on-the-go with PHY, plus three high-speed USB hosts, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100 Ethernet controller, and a variety of other popular interfaces (PATA, UART, I^2C, and I^2S serial audio, among others).
- Automotive environment support—Includes interfaces such as two CAN ports, an MLB port, an ESAI audio interface, and an asynchronous sample rate converter for multichannel/multisource audio.
- Advanced security—The i.MX53xA processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. For detailed information about the i.MX53xA security features contact a Freescale representative.

The i.MX53xA application processor is a follow-on to the i.MX51xA, with improved performance, power efficiency, and multimedia capabilities.

1.1 Ordering Information

Table 1 provides ordering information.

Table 1. Ordering Information

Part Number	Mask Set	Features		Package[1]
PCIMX536AVV8B	N78C	800 MHz, full feature set	—	19 x 19 mm, 0.8 mm pitch BGA Case TEPBGA-2

[1] Case TEPBGA-2 is RoHS compliant, lead-free MSL (moisture sensitivity level) 3.

1.2 Features

The i.MX53xA multimedia applications processor (AP) is based on the ARM Platform, which has the following features:

- MMU, L1 instruction and L1 data cache
- Unified L2 cache
- Target frequency of the core (including Neon, VFPv3 and L1 cache): 800 MHz
- Neon coprocessor (SIMD media processing architecture) and vector floating point (VFP-Lite) coprocessor supporting VFPv3
- TrustZone

The memory system consists of the following components:

- Level 1 cache:
  - Instruction (32 Kbyte)
  - Data (32 Kbyte)
- Level 2 cache:
  - Unified instruction and data (256 Kbyte)
- Level 2 (internal) memory:
  - Boot ROM, including HAB (64 Kbyte)
  - Internal multimedia/shared, fast access RAM (128 Kbyte)
  - Secure/non-secure RAM (16 Kbyte)
- External memory interfaces:
  - 16/32-bit DDR2-800, LV-DDR2-800 or DDR3-800 up to 2 Gbyte
  - 32bit LPDDR2
  - 8/16-bit NAND SLC/MLC Flash, up to 66 MHz, 4/8/14/16-bit ECC
  - 8,16-bit NOR Flash, PSRAM & cellular RAM.
  - 32-bit multiplexed mode NOR Flash, PSRAM & cellular RAM.
  - 8-bit Asynchronous (DTACK mode) EIM interface.

  - All EIM pins are muxed on other interfaces (data with NFC pins). I/O muxing logic selects EIM port, as primary muxing at system boot.
  - Samsung OneNAND™ and managed NAND including eMMC up to rev 4.4 (in muxed I/O mode)

The i.MX53xA system is built around the following system on chip interfaces:

- 64-bit AMBA AXI v1.0 bus—used by ARM platform, multimedia accelerators (such as VPU, IPU, GPU3D, GPU2D) and the external memory controller (EXTMC) operating at 200 MHz.
- 32-bit AMBA AHB 2.0 bus—used by the rest of the bus master peripherals operating at 133 MHz.
- 32-bit IP bus—peripheral bus used for control (and slow data traffic) of the most system peripheral devices operating at 66 MHz.

The i.MX53xA makes use of dedicated hardware accelerators to achieve state-of-the-art multimedia performance. The use of hardware accelerators provides both high performance and low power consumption while freeing up the CPU core for other tasks.

The i.MX53xA incorporates the following hardware accelerators:

- VPU, version 3—video processing unit
- GPU3D—3D graphics processing unit, OpenGL ES 2.0, version 3, 33 Mtri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance, 256 Kbyte RAM memory
- GPU2D—2D graphics accelerator, OpenVG 1.1, version 1, 200 Mpix/s performance,
- IPU, version 3M—image processing unit
- ASRC—asynchronous sample rate converter

The i.MX53xA includes the following interfaces to external devices:

NOTE

Not all interfaces are available simultaneously, depending on I/O multiplexer configuration.

- Hard disk drives:
  - PATA, up to U-DMA mode 5, 100 MByte/s
  - SATA I, 1.5 Gbps
- Displays:
  - Five interfaces available. Total rate of all interfaces is up to 180 Mpixels/s, 24 bpp. Up to two interfaces may be active at once.
  - Two parallel 24-bit display ports. The primary port is up to 165 Mpix/s (for example, UXGA @ 60 Hz).
  - LVDS serial ports: one dual channel port up to 165 Mpix/s or two independent single channel ports up to 85 MP/s (for example, WXGA @ 60 Hz) each.
  - TV-out/VGA port up to 150 Mpix/s (for example, 1080p60).
- Camera sensors:
  - Two parallel 20-bit camera ports. Primary up to 180-MHz peak clock frequency, secondary up to 120-MHz peak clock frequency.

- Expansion cards:
  - Four SD/MMC card ports: three supporting 416 Mbps (8-bit i/f) and one enhanced port supporting 832 Mbps (8-bit, eMMC 4.4).
- USB
  - High-speed (HS) USB 2.0 OTG (up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - High-speed host with integrated on-chip high-speed PHY
    - Two high-speed hosts for external HS/FS transceivers through ULPI/serial, support IC-USB
- Automotive environment interfaces:
  - Two controller area network (FlexCAN) interfaces, 1 Mbps each
  - Media local bus or MediaLB (MLB) provides interface to most networks (50 Mbps)
  - Enhanced serial audio interface (ESAI), up to 1.4 Mbps each channel
- Miscellaneous interfaces:
  - One-wire (OWIRE) port
  - Three I2S/SSI/AC97ports, supporting up to 1.4 Mbps, each connected to audio multiplexer (AUDMUX) providing four external ports.
  - Five UART RS232 ports, up to 4.0 Mbps each. One supports 8-wire, the other four support 4-wire.
  - Two high speed enhanced CSPI (ECSPI) ports plus one CSPI port
  - Three I^2C ports, supporting 400 kbps
  - Fast Ethernet controller, IEEE1588 V1 compliant, 10/100 Mbps
  - Sony Phillips Digital Interface (SPDIF), Rx and Tx
  - Key pad port (KPP)
  - Two pulse-width modulators (PWM)
  - GPIO with interrupt capabilities
  - Secure JTAG controller (SJC)

The system supports efficient and smart power control and clocking:

- Power gating SRPG (State Retention Power Gating) for ARM core and Neon
- Support for various levels of system power modes
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip oscillator amplifier supporting 32.768 kHz external crystal
- On-chip LDO voltage regulators for PLLs

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on)

- Secure JTAG controller (SJC)—Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features
- Secure real-time clock (SRTC)—Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches
- Real-time integrity checker, version 3 (RTICv3)—RTIC type1, enhanced with SHA-256 engine
- SAHARAv4 Lite—Cryptographic accelerator that includes true random number generator (TRNG)
- Security controller, version 2 (SCCv2)—Improved SCC with AES engine, secure/non-secure RAM and support for multiple keys as well as TZ/non-TZ separation
- Central security unit (CSU)—Enhancement for the IIM (IC Identification Module). CSU is configured during boot by e-fuses, and determines the security level operation mode as well as the TrustZone (TZ) policy
- Advanced High Assurance Boot (A-HAB)—HAB with the next embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization

NOTE

The actual feature set depends on the part number as described in Table 1. Functions such as video hardware acceleration, 2D and 3D hardware graphics acceleration, and Macrovision™ video copy protection may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX53xA processor system.

2.1 Block Diagram

Figure 1 shows the functional modules in the i.MX53xA processor system.

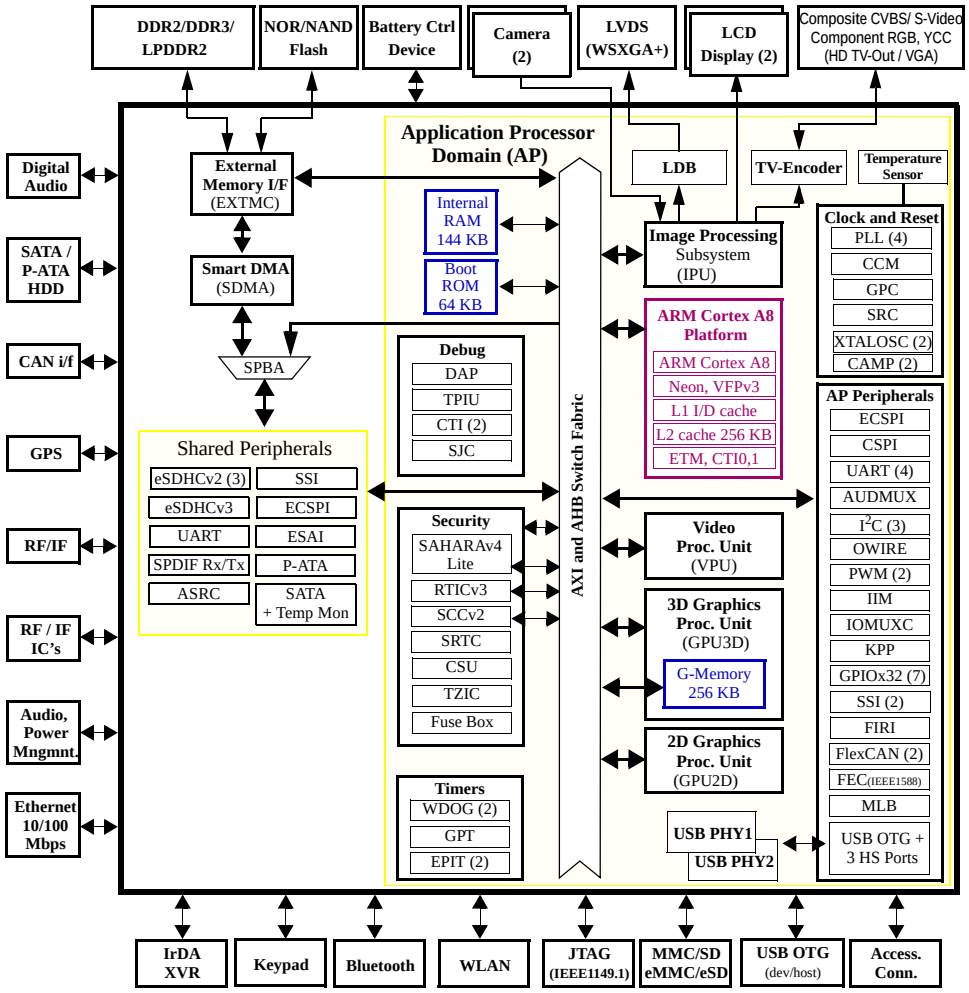


Figure 1. i.MX53xA System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (2) indicates two separate PWM peripherals.

3 Modules List

The i.MX53xA processor contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX53xA Digital and Analog Blocks

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM	ARM Platform	ARM	The ARM Cortex A8™ Platform consists of the ARM processor version r2p5 (with TrustZone) and its essential sub-blocks. It contains the 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, Level 2 cache controller and a 256 Kbyte L2 cache. The platform also contains an event monitor and debug modules. It also has a NEON coprocessor with SIMD media processing architecture, a register file with 32/64-bit general-purpose registers, an integer execute pipeline (ALU, Shift, MAC), dual single-precision floating point execute pipelines (FADD, FMUL), a load/store and permute pipeline and a non-pipelined vector floating point (VFP Lite) coprocessor supporting VFPv3.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The asynchronous sample rate converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about –120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Multiplexer	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports (three internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CAMP-1 CAMP-2	Clock Amplifier	Clocks, Resets, and Power Control	Clock amplifier
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, as well as for system power management. The system includes four PLLs.
CSPI ECSPI-1 ECSPI-2	Configurable SPI, Enhanced CSPI	Connectivity Peripherals	Full-duplex enhanced synchronous serial interface, with data rates 16-60 Mbit/s. It is configurable to support master/slave modes. In Master mode it supports four slave selects for multiple peripherals.
CSU	Central Security Unit	Security	The central security unit (CSU) is responsible for setting comprehensive security policy within the i.MX53xA platform, and for sharing security information between the various security modules. The security control registers (SCR) of the CSU are set during boot time by the high assurance boot (HAB) code and are locked to prevent further writing.

Table 2. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DEBUG	Debug System	System Control	The debug system provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView). Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, three cross-system triggers (CTI), counters, and sequencers. debug access port (DAP) —The DAP provides real-time access for the debugger without halting the core to system memory, peripheral register, debug configuration registers and JTAG scan chains.
EXTMC	External Memory Controller	Connectivity Peripherals	The EXTMC is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels, fast memories (DDR2/DDR3/LPDDR2) channel, slow memories (NOR-FLASH / PSRAM / NAND-FLASH etc.) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) channel. In order to increase the bandwidth performance, the EXTMC separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses. EXTMC Features: • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (read or write) was the last access • Flexible bank interleaving • Support 16/32-bit DDR2-800 or DDR3-800 or LPDDR2. • Support up to 2 GByte DDR memories. • Support NFC, EIM signal muxing scheme. • Support 8/16/32-bit Nor-Flash/PSRAM memories (sync and async operating modes), at slow frequency. (8-bit is not supported on D[23]-D[16]). • Support 4/8/14/16-bit ECC, page sizes of 512-B, 2-KB and 4-KB Nand-Flash (including MLC) • Multiple chip selects (up to 4). • Enhanced DDR memory controller, supporting access latency hiding • Support watermark for security (internal and external memories)
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI has 12 pins for data and clocking connection to external devices.

Table 2. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ESDHCV3-3	Ultra-High-Speed eMMC / SD Host Controller	Connectivity Peripherals	Ultra high-speed eMMC / SD host controller, enhanced to support eMMC 4.4 standard specification, for 832 MBps. • Port 3 is specifically enhanced to support eMMC 4.4 specification, for double data rate (832 Mbps, 8-bit port). ESDHCV3 is backward compatible to ESDHCV2 and supports all the features of ESDHCV2 as described below.
ESDHCV2-1 ESDHCV2-2 ESDHCv2-4	Enhanced Multi-Media Card / Secure Digital Host Controller		Enhanced multimedia card / secure digital host controller • Ports 1, 2, and 4 are compatible with the “MMC System Specification” version 4.3, full support and supporting 1, 4 or 8-bit data. The generic features of the eSDHCv2 module, when serving as SD / MMC host, include the following: • Can be configured either as SD / MMC controller • Supports eSD and eMMC standard, for SD/MMC embedded type cards • Conforms to SD Host Controller Standard Specification, version 2.0, full support. • Compatible with the SD Memory Card Specification, version 1.1 • Compatible with the SDIO Card Specification, version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: - SD/SDIO 1-bit, 4-bit - MMC 1-bit, 4-bit, 8-bit • Full/high speed mode. • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using 4 parallel data lines • Up to 416 Mbps data transfer for MMC cards using 8 parallel data lines
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet media access controller (MAC) is designed to support both 10 Mbps and 100 Mbps Ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX53xA also consists of HW assist for IEEE1588™ standard. See, TSU and CE_RTC (IEEE1588) section for more details.
FIRI	Fast Infrared Interface	Connectivity Peripherals	Fast infrared interface
FLEXCAN-1 FLEXCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The controller area network (CAN) protocol was primarily, but not exclusively, designed to be used as a vehicle serial data bus. Meets the following specific requirements of this application: real-time processing, reliable operation in the EXTMC environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN is a full implementation of the CAN protocol specification, Version 2.0 B (ISO 11898), which supports both standard and extended message frames at 1 Mbps.

Table 2. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3D	Graphics Processing Unit	Multimedia Peripherals	The GPU, version 3, provides hardware acceleration for 2D and 3D graphics algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution. It supports color representation up to 32 bits per pixel. GPU enables high-performance mobile 3D and 2D vector graphics at rates up to 33 Mtriangles/s, 200 Mpix/s, 800 Mpix/s (z).
GPU2D	Graphics Processing Unit-2D	Multimedia Peripherals	The GPU2D version 1, provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution.
I2C-1 I2C-2 I2C-3	I^2C Controller	Connectivity Peripherals	I^2C provides serial interface for controlling peripheral devices. Data rates of up to 400 kbps are supported.
IIM	IC Identification Module	Security	The IC identification module (IIM) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (e-Fuses). The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements not requiring non-volatility. The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals. The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module. IIM interfaces to the electrical fuse array (split to banks). Enables to set up boot modes, security levels, security keys and many other system parameters. i.MX53A consists of 4 x 256-bit + 1x 128-bit fuse-banks (total 1152 bits) through IIM interface.

Table 2. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
IPU	Image Processing Unit	Multimedia Peripherals	Version 3M IPU enables connectivity to displays, relevant processing and synchronization. It supports two display ports and two camera ports, through the following interfaces: • Legacy parallel interfaces • Single/dual channel LVDS display interface • Analog TV or VGA interfaces The processing includes: • Image enhancement—color adjustment and gamut mapping, gamma correction and contrast enhancement • Video/graphics combining • Support for display backlight reduction • Image conversion—resizing, rotation, inversion and color space conversion • Hardware de-interlacing support • Synchronization and control capabilities, allowing autonomous operation.
KPP	Keypad Port	Connectivity Peripherals	The KPP supports an 8 × 8 external keypad matrix. The KPP features are as follows: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS display bridge is used to connect the IPU (image processing unit) to external LVDS display interface. LDB supports two channels; each channel has following signals: • 1 clock pair • 4 data pairs On-chip differential drivers are provided for each pair.
MLB	Media local bus—MediaLB	Connectivity/ Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardize MediaLB protocol (up to 50 Mbps).
OWIRE	One-Wire Interface	Connectivity Peripherals	One-wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example, Dallas DS2502.
PATA	Parallel ATA	Connectivity Peripherals	The PATA block is a AT attachment host interface. Its main use is to interface with hard disk drives and optical disc drives. It interfaces with the ATA-6 compliant device over a number of ATA signals. It is possible to connect a bus buffer between the host side and the device side.
PWM-1 PWM-2	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound.

Table 2. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
INTRAM	Internal RAM	Internal Memory	Internal RAM, shared with VPU. The on-chip memory controller (OCRAM) module, is an interface between the system's AXI bus, to the internal (on-chip) SRAM memory module. It is used for controlling the 128 KB multimedia RAM, through a 64-bit AXI bus.
BOOTROM	Boot ROM	Internal Memory	Supports secure and regular boot modes. The ROM controller supports ROM patching.
RTIC	Real Time Integrity Checker	Security	Protecting read only data from modification is one of the basic elements in trusted platforms. The run-time integrity checker, version 3 (RTIC) block is a data-monitoring device responsible for ensuring that the memory content is not corrupted during program execution. The RTIC mechanism periodically checks the integrity of code or data sections during normal OS run-time execution without interfering with normal operation. The purpose of the RTIC is to ensure the integrity of the peripheral memory contents, protect against unauthorized external memory elements replacement and assist with boot authentication.
SAHARA	SAHARA Security Accelerator	Security	SAHARA (symmetric/asymmetric hashing and random accelerator), version 4, is a security coprocessor. It implements symmetric encryption algorithms, (AES, DES, 3DES, RC4 and C2), public key algorithms (RSA and ECC), hashing algorithms (MD5, SHA-1, SHA-224 and SHA-256), and a hardware true random number generator. It has a slave IP Bus interface for the host to write configuration and command information, and to read status information. It also has a DMA controller, with an AHB bus interface, to reduce the burden on the host to move the required data to and from memory.
SATA	Serial ATA	Connectivity Peripherals	SATA HDD interface, includes the SATA controller and the PHY. It is a complete mixed-signal IP solution for SATA HDD connectivity.
SCCv2	Security Controller, ver. 2	Security	The security controller is a security assurance hardware module designed to safely hold sensitive data, such as encryption keys, digital right management (DRM) keys, passwords and biometrics reference data. The SCCv2 monitors the system's alert signal to determine if the data paths to and from it are secure, that is, it cannot be accessed from outside of the defined security perimeter. If not, it erases all sensitive data on its internal RAM. The SCCv2 also features a key encryption module (KEM) that allows non-volatile (external memory) storage of any sensitive data that is temporarily not in use. The KEM utilizes a device-specific hidden secret key and a symmetric cryptographic algorithm to transform the sensitive data into encrypted data.

Table 2. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off loading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (copy mode) • Up to 8-word buffer for configurable burst transfers to / from the EXTMC • Support of byte swapping and CRC calculations • A library of scripts and API is available
SECRAM	Secure / Non-secure RAM	Internal Memory	Secure / non-secure Internal RAM, controlled by SCC.
SJC	Secure JTAG Interface	System Control Peripherals	JTAG manipulation is a known hacker's method of executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The JTAG port provides a debug access to several hardware blocks including the ARM processor and the system bus. The JTAG port must be accessible during platform initial laboratory bring-up, manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. However, in order to properly secure the system, unauthorized JTAG usage should be strictly forbidden. In order to prevent JTAG manipulation while allowing access for manufacturing tests and software debugging, the i.MX53xA processor incorporates a mechanism for regulating JTAG access. SJC provides four different JTAG security modes that can be selected through an e-fuse configuration.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (shared peripheral bus arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SPDIF	Sony Philips Digital Interface	Multimedia Peripherals	A standard digital audio transmission protocol developed jointly by the Sony and Philips corporations. Both transmitter and receiver functionalists are supported.

Table 2. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SRTC	Secure Real Time Clock	Security	The SRTC incorporates a special system state retention register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC_POW. The NVCC_SRTC_POW can be energized separately even if all other supply rails are shut down. The power for this block comes from NVCC_SRTC_POW supply. When this supply is driven by the MC13892 power management controller, this block can be power backed up through the coin-cell feature of the MC13892. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR mark the event (security violation indication).
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX53A processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously.
IPTP	IEEE1588 Precision Time Protocol	Connectivity Peripherals	The IEEE 1588-2002 (version 1) standard defines a precision time protocol (PTP) - which is a time-transfer protocol that enables synchronization of networks (for example, Ethernet), to a high degree of accuracy and precision. The IEEE1588 hardware assist is composed of the two blocks: time stamp unit and real time clock, which provide the timestamping protocol's functionality, generating and reading the needed timestamps. The hardware-assisted implementation delivers more precise clock synchronization at significantly lower CPU load compared to purely software implementations.
Temperature Monitor	(Part of SATA Block)	System Control Peripherals	The temperature sensor is an internal module to the i.MX53xA that monitors the die temperature. The monitor is capable in generating SW interrupt, or trigger the CCM, to reduce the core operating frequency.
TVE	TV Encoder	Multimedia	The TV encoder, version 2.1 is implemented in conjunction with the image processing unit (IPU) allowing handheld devices to display captured still images and video directly on a TV or LCD projector. It supports composite PAL/NTSC, VGA, S-video, and component up to HD1080p analog video outputs.
TZIC	TrustZone Aware Interrupt Controller	ARM/Control	The TrustZone interrupt controller (TZIC) collects interrupt requests from all i.MX53xA sources and routes them to the ARM core. Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported.

Table 2. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UART blocks supports the following serial data transmit/receive protocols and configurations: • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USB	USB Controller	Connectivity Peripherals	USB supports USB2.0 480 MHz, and contains: • One high-speed OTG sub-block with integrated HS USB PHY • One high-speed host sub-block with integrated HS USB PHY • Two identical high-speed Host modules The high-speed OTG module, which is internally connected to the HS USB PHY, is equipped with transceiver-less logic to enable on-board USB connectivity without USB transceivers All the USB ports are equipped with standard digital interfaces (ULPI, HS IC-USB) and transceiver-less logic to enable onboard USB connectivity without USB transceivers.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU) version 3, which covers many SD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing such as rotation and mirroring. VPU Features: • MPEG-2 decode, Mail-High profile, up to 1080i/p resolution, 40 Mbps bit rate • MPEG4/XviD decode, SP/ASP profile, up to 1080 i/p resolution, 40 Mbps bit rate • H.263 decode, P0/P3 profile, up to 16CIF resolution, 20 Mbps bit rate • Sorenson H.263 decode, 4CIF resolution, 8 Mbps bit rate • H.264 decode, BP/MP/HP profile, up to 1080 i/p resolution, 40 Mbps bit rate • VC1 decode, SP/MP/AP profile, up to 1080 i/p resolution, 40 Mbps bit rate • RV10 decode, 8/9/2010 profile, up to 1080 i/p resolution, 40 Mbps bit rate • DivX decode, 3/4/5/6 profile, up to 1080 i/p resolution, 40 Mbps bit rate • MJPEG decode, Baseline profile, up to 8192 x 8192 resolution, 40 Mpixel/s bit rate for 4:4:4 format • MPEG2[1] encode, Main-Main profile, up to D1 resolution, 15 Mbps bit rate • MPEG4 encode, Simple profile, up to 720p resolution, 12 Mbps bit rate[2] • H.263 encode, P0/P3 profile, up to 4CIF resolution, 8 Mbps bit rate[2] • H.264 encode, Baseline profile, up to 720p resolution, 14 Mbps bit rate[2] • MJPEG encode, Baseline profile, up to 8192 x 8192 resolution, 80 Mpixel/s bit rate for 4:2:2 format
WDOG-1	Watch Dog	Timer Peripherals	The watch dog timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.

Table 2. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. This situation should be avoided, as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
XTALOSC	24 MHz Crystal Oscillator	Clocking	Provides a crystal oscillator amplifier that supports a 24-MHz external crystal
XTALOSC_ 32K	32.768 KHz Crystal Oscillator I/F	Clocking	Provides a crystal oscillator amplifier that supports a 32.768-kHz external crystal.

[1] Video partially performed in hardware accelerator (70%) and partially in software.

[2] VPU can generate higher bit rate than the maximum specified by the corresponding standard.

3.1 Special Signal Considerations

Special signal consideration information is contained in Chapter 1 of i.MX53 System Development User's Guide.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in i.MX53xA Reference Manual.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX53xA processor.

NOTE

This electrical specification is preliminary. These specifications are not fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after thorough characterization and device qualifications have been completed.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 3 for a quick reference to the individual tables and sections.

Table 3. i.MX53xA Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	Table 4 on page 18
Package Thermal Resistance Data	Table 5 on page 19
i.MX53xA Operating Ranges	Table 6 on page 19
External Clock Sources	Table 7 on page 22
Maximal Supply Currents	Table 8 on page 22
USB Interface Current Consumption	Table 9 on page 24

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 6 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 4. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Peripheral Core Supply Voltage	VCC	–0.3	1.35	V
ARM Core Supply Voltage	VDDGP	–0.3	1.35	V
Supply Voltage UHVIO	Supplies denoted as I/O Supply	–0.5	3.6	V
Supply Voltage for non UHVIO	Supplies denoted as I/O Supply	–0.5	3.3	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	–0.3	3.63[1]	V
Input/Output Voltage Range	V_{in}/V_{out}	–0.5	OVDD +0.3[2]	V
ESD Damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage Temperature Range	$T_{STORAGE}$	–40	150	°C

1 USB_DN and USB_DP can tolerate 5 V for up to 24 hours.

2 The term OVDD in this section refers to the associated supply rail of an input or output. The association is described in Table 112 on page 159. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance

Table 5 provides the package thermal resistance data.

Table 5. Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	28	°C/W
Junction to Ambient (natural convection)[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	16	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	21	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	6	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	4	°C/W
Junction to Package Top (natural convection)[6]	—	Ψ_{JT}	4	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.1.3 Operating Ranges

Table 6 provides the operating ranges of i.MX53xA processor.

Table 6. i.MX53xA Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP	ARM core supply voltage $f_{ARM} \leq 800$ MHz	1.05	1.1	1.15	V
	ARM core supply voltage Stop mode	0.8	0.85	1.15	V
VCC	Peripheral supply voltage	1.25	1.3	1.35	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.35	V
VDDA[3]	Memory arrays voltage	1.25	1.30	1.35	V
	Memory arrays voltage—Stop mode	0.9	0.95	1.35	V

Table 6. i.MX53xA Operating Ranges (continued)

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDAL1[3]	L1 Cache Memory arrays voltage	1.25	1.30	1.35	V
	L1 Cache Memory arrays voltage—Stop mode	0.9	0.95	1.35	V
VDD_DIG_PLL[4]	PLL Digital supplies—external regulation option	1.25	1.3	1.35	V
VDD_ANA_PLL[5]	PLL Analog supplies—external regulator option	1.75	1.8	1.95	V
NVCC_CKIH	ESD protection of the CKIH pins, FUSE read Supply and 1.8V bias for the UHVIO pads	1.65	1.8	1.95	V
NVCC_LCD NVCC_JTAG	GPIO digital power supplies	1.65	1.8 or 2.775	3.1	V
NVCC_LVDS	LVDS interface Supply	2.25	2.5	2.75	V
NVCC_LVDS_BG	LVDS Band Gap Supply	2.25	2.5	2.75	V
NVCC_EMI_DRAM	DDR Supply DDR2 range	1.7	1.8	1.9	V
	DDR Supply LPDDR2 range	1.14	1.2	1.3	
	DDR Supply LV-DDR2 range	1.47	1.55	1.63	
		1.42	1.5	1.58	
	DDR Supply DDR3 range	1.42	1.5	1.58	
VDD_FUSE[6]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V
NVCC_NANDF NVCC_SD1 NVCC_SD2 NVCC_PATA NVCC_KEYPAD NVCC_GPIO NVCC_FEC NVCC_EIM_MAIN NVCC_EIM_SEC NVCC_CSI	Ultra High voltage I/O (UHVIO) supplies				V
	UHVIO_L	1.65	1.8	1.95	
	UHVIO_H	2.5	2.775	3.1	
	UHVIO_UH	3.0	3.3	3.6	
TVDAC_DHVDD[7] TVDAC_AHVDDRGB[7]	TVE digital and analog power supply, TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel	2.69	2.75	2.91	V
	For GPIO use only, when TVE is not in use	1.65	1.8 or 2.775	3.1	V
NVCC_SRTC_POW	SRTC Core and slow I/O Supply (GPIO)[8]	1.25	1.3	1.35	V
NVCC_RESET	LVIO	1.65	1.8 or 2.775	3.1	V
USB_H1_VDDA25 USB_OTG_VDDA25 NVCC_XTAL	USB_PHY analog supply, oscillator amplifier analog supply[9]	2.25	2.5	2.75	V
USB_H1_VDDA33 USB_OTG_VDDA33	USB PHY I/O analog supply	3.0	3.3	3.6	V

Table 6. i.MX53xA Operating Ranges (continued)

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VBUS	See Table 4 on page 18 and Table 104 on page 151 for details. Note that this is not a power supply.	—	—	—	—
VDD_REG[10]	Power supply input for the integrated linear regulators	2.37	2.5	2.63	V
VP	SATA PHY core power supply.	1.25	1.3	1.35	V
VPH	SATA PHY I/O supply voltage	2.25	2.5	2.75	V
T_J	Junction Temperature	–40	105[11]	125	°C

1 Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

2 The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

3 VDDA and VDDAL1 can be driven by the VDD_DIG_PLL internal regulator using external connections. When operating in this configuration, the regulator is still operating at the default 1.2V, as bootup start. This is acceptable for boot modes when connecting any or all of these supplies to the internal on-die LDO regulator.

During bootup initialization, software should increase this regulator voltage to match VCC (1.3V nominal) in order to reduce internal leakage current.

4 By default, VDD_DIG_PLL is driven from internal on-die 1.2 V linear regulator (LDO). In this case, there is no need driving this supply externally. LDO output to VDD_DIG_PLL should be configured by software after power-up to 1.3 V output. A bypass capacitor of minimal value 22 μF should be connected to this pad in any case whether it is driven internally or externally. Use of the on-chip LDO is preferred. See i.MX53 System Development User's Guide.

5 By default, the VDD_ANA_PLL is driven from internal on-die 1.8 V linear regulator (LDO). In this case there is no need driving this supply externally. A bypass capacitor of minimal value 22 μF should be connected to this pad in any case whether it is driven internally or externally. Use of the on-chip LDO is preferred. See i.MX53 System Development User's Guide.

6 In case the VDD_FUSE is kept powered on during Fuse Read mode, the efuse_prog_supply_gate bit in CCM_CGPR register should be kept low, to avoid the possibility of inadvertently blowing fuses. Alternately, VDD_FUSE can be ground or left floating, when not in Fuse Write mode.

7 If not using TVE module or other pads in this power domain for the product, the TVDAC_DHVDD and TVDAC_AHVDDRGB can remain floating.

8 GPIO pad operational at low frequency

9 The analog supplies should be isolated in the application design. Use of series inductors is recommended.

10 VDD_REG is power supply input for the integrated linear regulators of VDD_ANA_PLL and VDD_DIG_PLL when they are configured to the internal supply option. VDDR_REG still has to be tied to 2.5 V supply when VDD_ANA_PLL and VDD_DIG_PLL are configured for external power supply mode although in this case it is not used as supply source.

11 Lifetime of 43,800 hours based on 105 C junction temperature at nominal supply voltages.

4.1.4 External Clock Sources

The i.MX53xA device has four external input system clocks, a low frequency (CKIL), a high frequency (XTAL), and two general purpose CKIH1 and CKIH2 clocks.

The CKIL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

CKIH1 and CKIH2 provide additional clock source option for peripherals that require specific and accurate frequencies.

Table 7 shows the interface frequency requirements.

Table 7. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
CKIL Oscillator[1]	f_{ckil}	—	32.768[2]/32.0	—	kHz
CKIH1, CKIH2 Operating Frequency	f_{ckih1}, f_{ckih2}	See Table 31, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 44			MHz
XTAL Oscillator	f_{xtal}	22	24	27	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 Recommended nominal frequency 32.768 kHz.

4.1.5 Maximal Supply Currents

Table 8 represents the maximal momentary current transients on power lines, and should be used for power supply selection. Maximal currents higher by far than the average power consumption of typical use cases. For typical power consumption information, see i.MX53xA power consumption application note.

Table 8. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDGP	800MHz ARM clock.	1450	mA
VCC		800	mA
VDDA+VDDAL1		100	mA
VDD_DIG_PLL		10	mA
VP		20	mA
VDD_ANA_PLL		10	mA
MVCC_XTAL		25	mA
VDD_REG		325	mA
VDD_FUSE	Fuse Write Mode operation	60	mA
NVCC_EMI_DRAM	1.8v (DDR2)	800	mA
	1.5v (DDR3)	650	mA
	1.2v (LPDDR2)	250	mA
TVDAC_DHVDD + TVDAC_AHVDDRGB		200	mA

Table 8. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_SRTC_POW		<1	mA
USB_H1_VDDA25 + USB_OTG_VDDA25		50	mA
USB_H1_VDDA33 + USB_OTG_VDDA33		20	mA
VPH		60	mA
NVCC_CKIH		Use maximal IO Eq[1], N=4	
NVCC_CSI		Use maximal IO Eq[1], N=20	
NVCC_EIM_MAIN		Use maximal IO Eq[1], N=39	
NVCC_EIM_SEC		Use maximal IO Eq[1], N=16	
NVCC_EMI_DRAM		Use maximal IO Eq[1], N=78	
NVCC_FEC		Use maximal IO Eq[1], N=11	
NVCC_GPIO		Use maximal IO Eq[1], N=13	
NVCC_JTAG		Use maximal IO Eq[1], N=6	
NVCC_KPAD		Use maximal IO Eq[1], N=11	
NVCC_LCD		Use maximal IO Eq[1], N=29	
NVCC_LVDS		Use maximal IO Eq[1], N=20	
NVCC_LVDS_BG		Use maximal IO Eq[1], N=1	
NVCC_NANDF		Use maximal IO Eq[1], N=8	
NVCC_PATA		Use maximal IO Eq[1], N=29	
NVCC_REST		Use maximal IO Eq[1], N=5	
NVCC_SD1		Use maximal IO Eq[1], N=6	
NVCC_SD2		Use maximal IO Eq[1], N=6	
NVCC_XTAL		Use maximal IO Eq[1], N=2	

[1] General Equation for estimated, maximal power consumption of an IO power supply:

Imax = N * C * V * (0.5 * F)

Where:

N - Number of IO pins supplies by the power line

C - Equivalent external capacitive load

V - IO voltage

(0.5 * F) - Data change rate. Up to 0.5 of the clock rate (F).

4.1.6 xAUSB-OH-3 (OTG + 3 Host ports) Module and the Two USB PHY (OTG and H1) Current Consumption

Table 9 shows the USB interface current consumption.

Table 9. USB Interface Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog Supply 3.3 V USB_H1_VDDA33 USB_OTG_VDDA33	Full Speed	RX	5.5	6	mA
		TX	7	8	
	High Speed	RX	5	6	
		TX	5	6	
Analog Supply 2.5 V USB_H1_VDDA25 USB_OTG_VDDA25	Full Speed	RX	6.5	7	mA
		TX	6.5	7	
	High Speed	RX	12	13	
		TX	21	22	
Digital Supply VCC (1.2 V)	Full Speed	RX	8	—	mA
		TX	8	—	
	High Speed	RX	8	—	
		TX	8	—	
USB_H1_VDDA33 + USB_OTG_VDDA33 + USB_H1_VDDA25 + USB_OTG_VDDA25 + VCC	Suspend		—	—	µA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX53xA processor (worst-case scenario)

4.2.1 Power-Up Sequence

The following observations should be considered:

- The consequent steps in power up sequence should not start before the previous step supplies have been stabilized within 90-110% of their nominal voltage, unless stated otherwise.

- NVCC_SRTC_POW should remain powered ON continuously, to maintain internal real-time clock status. Otherwise, it has to be powered ON together with VCC, or preceding VCC.
- The VCC should be powered ON together, or any time after NVCC_SRTC_POW.
- NVCC_CKIH should be powered ON after VCC is stable and before other IO supplies (NVCC_xxx) are powered ON.
- IO Supplies (NVCC_xxx) below or equal to 2.8 V nom./3.1 V max. should not precede NVCC_CKIH. They can start powering ON during NVCC_CKIH ramp-up, before it is stabilized. Within this group, the supplies can be powered-up in any order.
- IO Supplies (NVCC_xxx) above 2.8 V nom./3.1 V max. should be powered ON only after NVCC_CKIH is stable.
- In case VDD_DIG_PLL and VDD_ANA_PLL are powered ON from internal voltage regulator (default case for i.MX53), there are no related restrictions on VDD_REG, as it is used as their internal regulators power source.
  If VDD_DIG_PLL and VDD_ANA_PLL are powered on externally, to reduce current leakage during the power-up, it is recommended to activate the VDD_REG before or at the same time with VDD_DIG_PLL and VDD_ANA_PLL. If this sequencing is not possible, make sure that the 2.5 V VDD_REG supply shut-off output impedance is higher than 1 kΩ when it is inactive.
- VDD_REG supply is required to be powered ON to enable DDR operation. It must be powered on after VCC and before NVCC_EMI_DRAM. The sequence should be:

  $$VCC \rightarrow VDD_REG \rightarrow NVCC_EMI_DRAM$$

- VDDA and VDDAL1 can be powered ON anytime before POR_B, regardless of any other power signal.
- VDDGP can be powered ON anytime before POR_B, regardless of any other power signal.
- VP and VPH can be powered up together, or anytime after, the VCC. VP and VPH should come before POR.
- TVDAC_DHVDD and TVDAC_AHVDDRGB should be powered from the same regulator. This is due to ESD diode protection circuit, that may cause current leakage if one of the supplies is powered ON before the other.

NOTE

The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage.

Figure 2 shows the power-up sequence diagram.

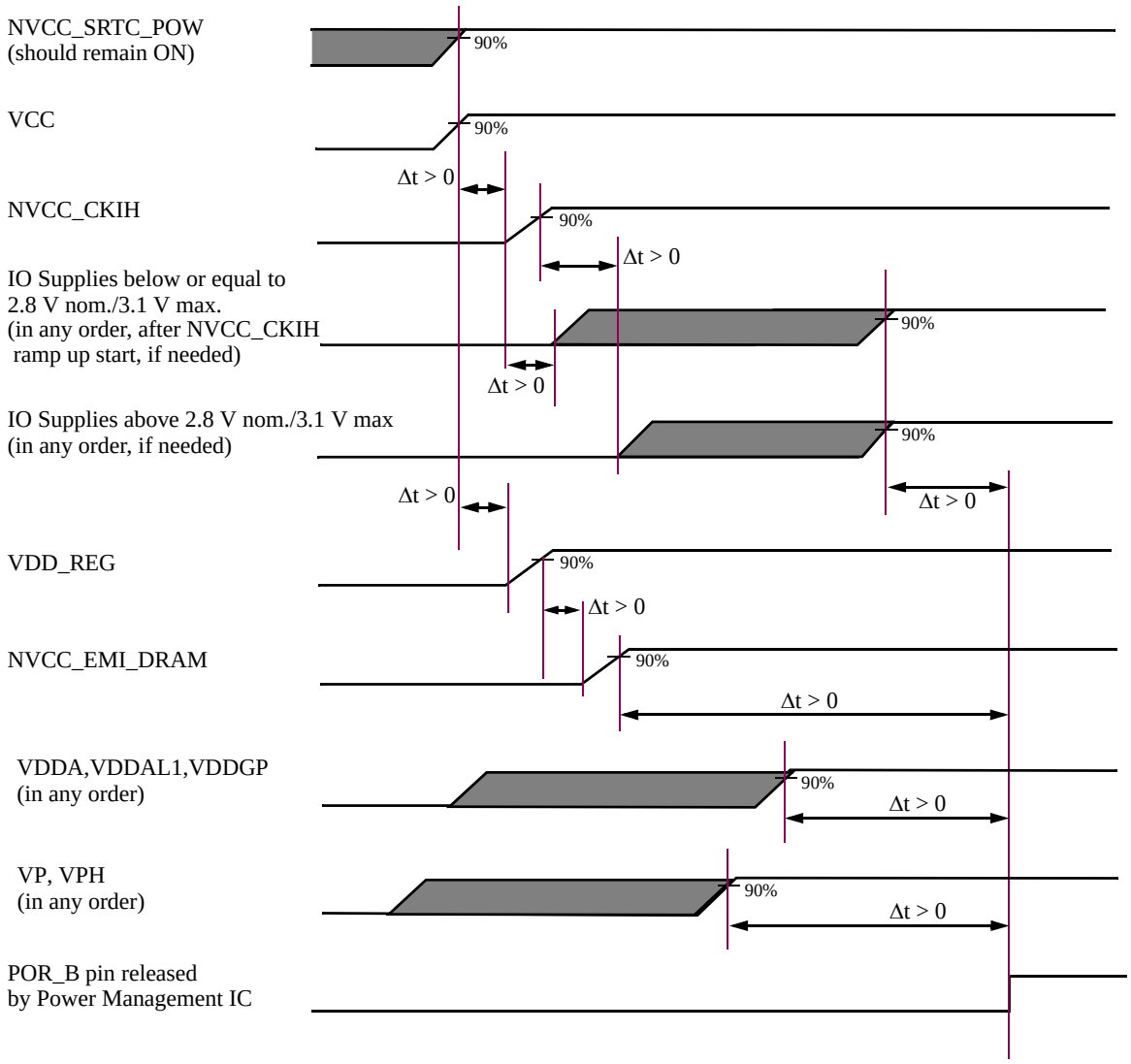


Figure 2. Power Up Detailed Sequence [1]

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the parts that use both 1.8 V and the 3.3 V supply).

1. If fuse writing is required, VDD_FUSE should be powered ON after NVCC_CKIH is stable.

4.2.2 Power-Down Sequence

Power-down sequence should follow one of the following two options:

Option 1: Switch all supplies down simultaneously with further free discharge. A deviation of few microseconds of actual power-down of the different power rails is acceptable.

Option 2: Switch down supplies, in any order, keeping the following rules:

- NVCC_CKIH must be powered down at the same time or after the UHVIO IO cell supplies. A deviation of few microseconds of actual power-down of the different power rails is acceptable.
- VDD_REG must be powered down at the same time or after NVCC_EMI_DRAM supply. A deviation of few microseconds of actual power-down of the different power rails is acceptable.
- If all of the following conditions are met:
  - 1. VDD_REG is powered down to 0V (Not Hi-Z)
  - 2. VDD_DIG_PLL and VDD_ANA_PLL are provided externally,
  - 3. VDD_REG is powered down before VDD_DIG_PLL and VDD_ANA_PLL

  Then the following rule should be kept: VDD_REG output impedance must be higher than 1 kΩ, when inactive.

4.2.3 Power Supplies Usage

- All IO pins should not be externally driven while the IO power supply for the pin (NVCC_xxx) is off. This can cause internal latch-up and malfunctions due to reverse current flows. For information about IO power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package Information and Contact Assignments.”
- If not using SATA interface and the embedded thermal sensor, the VP and VPH should be grounded. In particular, keeping VPH turned OFF while the VP is powered ON is not recommended and might lead to excessive power consumption.
- When internal clock source is used for SATA temperature monitor the USB_PHY supplies and PLL need to be active because they are providing the clock.
- If not using TVE the module, the TVDAC_DHVDD and TVDAC_AHVDDRGB can remain floating. If only the GPIO pads in TVDAC_AHVDDRGB domain are in use, the supplies can be set to GPIO pad voltage range (1.65 V to 3.1 V).

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2 and DDR3 modes
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output. The association is shown in Table 112.

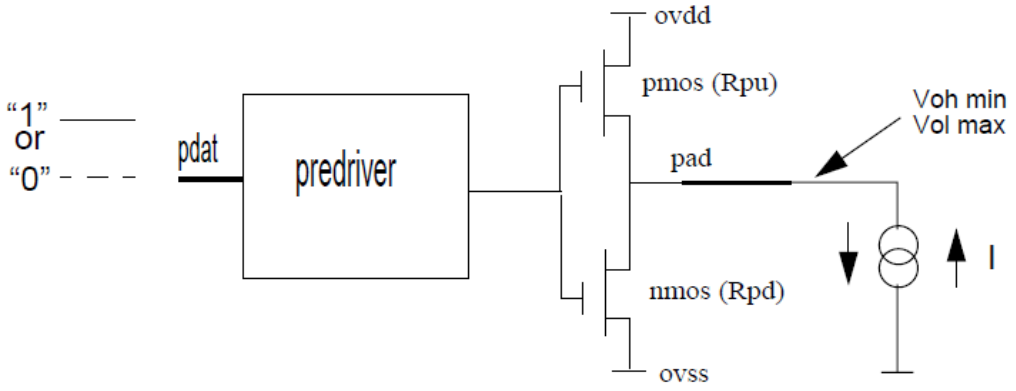


Figure 3. Circuit for Parameters Voh and Vol for IO Cells

4.3.1 General Purpose I/0 (GPIO) DC Parameters

The parameters in Table 10 are guaranteed per the operating ranges in Table 6, unless otherwise noted. Table 10 shows DC parameters for GPIO pads, operating at two supply ranges:

- 1.1 V to 1.3 V
- 1.65 V to 3.1 V

Table 10. GPIO I/O DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage[1]	Voh	Iout = –1 mA Iout= specified Ioh Drive	OVDD – 0.15 0.8*OVDD	—	—	V
Low-level output voltage[1]	Vol	Iout = 1 mA Iout= specified Iol Drive	—	—	0.15 0.2 × OVDD	V
High-level output current (1.1-1.3V OVDD)	Ioh	Vout = 0.8×OVDD Low drive Medium drive High drive Max drive	 –0.85 –1.7 –2.5 –3.4	—	—	mA
Low-level output current (1.1-1.3V OVDD)	Iol	Vout = 0.2×OVDD Low drive Medium drive High drive Max drive	 0.9 1.9 2.9 3.8	—	—	mA
High-level output current (1.65-3.1V OVDD)	Ioh	Vout = 0.8×OVDD Low drive Medium drive High drive Max drive	 –2.1 –4.2 –6.3 –8.4	—	—	mA

Table 10. GPIO I/O DC Electrical Characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low-level output current (1.65-3.1V OVDD)	Iol	Vout = 0.2×OVDD Low drive Medium drive High drive Max drive	 2.1 4.2 6.3 8.4	—	—	mA
High-Level DC input voltage[1, 2]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1, 2]	VIL	—	0	—	0.3 × OVDD	V
Input Hysteresis	VHYS	OVDD = 1.875 V OVDD = 2.775 V	0.25	0.34 0.45	—	V
Schmitt trigger VT+[2, 3]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[2, 3]	VT–	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	IIN	VI = 0 V VI = OVDD	1.7	—	250 120	nA
Input current (22 kΩ Pull-up)	IIN	VI = 0 V VI = OVDD	—	—	161 0.12	μA
Input current (47 kΩ Pull-up)	IIN	VI = 0 V VI = OVDD	—	—	76 0.12	μA
Input current (100 kΩ Pull-up)	IIN	VI = 0 V V I= OVDD	—	—	36 0.12	μA
Input current (100 kΩ Pull-down)	IIN	VI = 0 V VI = OVDD	—	—	0.25 36	μA
Keeper Circuit Resistance			—	125[4]	—	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4 Use an off-chip pull resistor of less than 60kΩ to override this keeper.

4.3.2 LPDDR2 I/O DC Parameters

The LPDDR2 I/O pads support DDR2/LVDDR2, LPDDR2, and DDR3 operational modes.

4.3.2.1 DDR2 Mode I/O DC Parameters

The DDR2 interface fully complies with JESD79-2E DDR2 JEDEC standard release April, 2008. The parameters in Table 11 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 11. DDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage[2]	Voh	—	0.9*OVDD	—	—	V
Low-level output voltage	Vol	—	—	—	0.1*OVDD	V
Output minimum Source Current[3]	Ioh	OVDD=1.7 V, Vout=1.42 V	–13.4	—	—	mA
Output min Sink Current[4]	Iol	OVDD=1.7 V, Vout=280 mV	13.4	—	—	mA
Input Reference Voltage	Vref		0.49*OVDD	0.5*OVDD	0.51*OVDD	
DC input High Voltage (data pins)	Vihd (dc)	—	Vref+0.125V	—	OVDD+0.3	V
DC input Low Voltage (data pins)	Vild (dc)	—	–0.3	—	Vref-0.125V	V
DC Input voltage range of each differential input[5]	Vin (dc)	—	–0.3	—	OVDD+0.3	V
DC Differential input voltage required for switching [6]	Vid(dc)	—	0.25	—	OVDD+0.6	V
Termination Voltage	Vtt	Vtt	Vref – 0.04	Vref	Vref + 0.04	V
Input current (no pull-up/down)[7]	Iin	VI = 0 V VI=OVDD	— —	0.07 2	5 360	nA
Keeper Circuit Resistance	—	—	—	125[8]	—	kΩ

1 Note that the JEDEC SSTL_18 specification (JESD8-15a) for a SSTL interface for class II operation supersedes any specification in this document.

2 OVDD is the I/O power supply (1.7 V–1.9 V for DDR2)

3 (Vout - OVDD) / Ioh must be less than 21 Ω for values of Vout between OVDD and OVDD-0.28 V.

4 Vout / Iol must be less than 21 Ω for values of Vout between 0 V and 280 mV.

5 Vin(dc) specifies the allowable DC voltage exertion of each differential input.

6 Vid(dc) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input level and Vcp is the “complementary” input level. The minimum value is equal to Vih(dc) -Vil(dc).

7 Typ condition: 1.8 V, and 25 °C. Max condition: 1.9 V, and 105 °C.

8 Use an off-chip pull resistor of less than 60kΩ to override this keeper.

4.3.2.2 LPDDR2 Mode I/O DC Parameters

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009.

Table 12. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	—	0.9*OVDD	—	—	V
Low-level output voltage	Vol	—	—	—	0.1*OVDD	V
Input Reference Voltage	Vref		0.49*OVDD	0.5*OVDD	0.51*OVDD	
DC input High Voltage	Vih(dc)	—	Vref+0.13V	—	OVDD	V

Table 12. LPDDR2 I/O DC Electrical Parameters[1] (continued)

DC input Low Voltage	Vil(dc)	—	OVSS	—	Vref-0.13V	V
Differential Input Logic High	Vih(diff)		0.26		See Note[2]	
Differential Input Logic Low	Vil(diff)		See Note[2]		-0.26	
Input current (no pull-up/down)	Iin	VI = 0 V VI=OVDD	— —	0.02 1.5	12.8 290	nA
Pull-up/Pull-down impedance Mismatch			-15		+15	%
240 Ohm unit calibration resolution					10	Ohm
Keeper Circuit Resistance	—	—	—	125[3]	—	kΩ

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

3 Use an off-chip pull resistor of less than 60kΩ to override this keeper.

4.3.2.3 DDR3 Mode I/O DC Parameters

The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. The parameters in Table 13 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 13. DDR3 I/O DC Electrical Parameters

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	—	0.8*OVDD[1]	—	—	V
Low-level output voltage	Vol	—	—	—	0.2*OVDD	V
DC input Logic High	VIH(dc)	—	Vref[2]+0.1	—	OVDD	V
DC input Logic Low	VIL(dc)	—	OVSS	—	Vref-0.1	V
Differential input Logic High	VIH(diff)	—	0.2	—	See Note[3]	V
Differential input Logic Low	VIL(diff)	—	See Note[3]	—	-0.2	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	—	—	—	0.67	V x nS
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	Vref	0.51*OVDD	V
Input current (no pull-up/down)	Iin	VI = 0 V VI=OVDD	— —	0.09 1.75	15 320	nA
Pull-up/Pull-down impedance mismatch	—	Minimum impedance configuration	—	—	3	Ω
240 Ω unit calibration resolution	—	—	—	—	10	Ω
Keeper Circuit Resistance	—	—	—	125[4]	—	kΩ

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3)

2 Vref – DDR3 external reference voltage

3 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4 Use an off-chip pull resistor of less than 60kΩ to override this keeper.

4.3.3 Low Voltage I/O (LVIO) DC Parameters

The parameters in Table 14 are guaranteed per the operating ranges in Table 6, unless otherwise noted. The LVIO pads operate only as inputs.

Table 14. LVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
High-Level DC input voltage[1, 2]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1, 2]	VIL	—	0	—	0.3 × OVDD	V
Input Hysteresis	VHYS	OVDD = 1.875 V OVDD = 2.775 V	0.35	0.62 1.27	—	V
Schmitt trigger VT+[2, 3]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[2, 3]	VT–	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	IIN	VI = 0 V VI = OVDD	—	1.7	250 120	nA
Input current (22 kΩ Pull-up)	IIN	VI = 0 V VI = OVDD	—	—	161 0.12	μA
Input current (47 kΩ Pull-up)	IIN	VI = 0 V VI = OVDD	—	—	76 0.12	μA
Input current (100 kΩ Pull-up)	IIN	VI = 0 V VI = OVDD	—	—	36 0.12	μA
Input current (100 kΩ Pull-down)	IIN	VI = 0 V VI = OVDD	—	—	0.25 36	μA
Keeper Circuit Resistance	—	OVDD = 1.875 V OVDD = 2.775 V	— —	125[4] 125	— —	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

3 Hysteresis of 350 mV is guaranteed over all operating conditions when hysteresis is enabled.

4 Use an off-chip pull resistor of less than 60kΩ to override this keeper.

4.3.4 Ultra-High Voltage I/O (UHVIO) DC Parameters

The parameters in Table 15 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 15. UHVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage[1]	Voh	Iout = –1mA Iout= specified Ioh Drive	OVDD–0.15 0.8 * OVDD	—	—	V
Low-level output voltage[1]	Vol	Iout = 1mA Iout= specified Ioh Drive	—	—	0.15 0.2 * OVDD	V
High-level output current, low voltage mode	Ioh_lv	Vout = 0.8 × OVDD Low Drive Medium Drive High Drive	 –2.2 –4.4 –6.6	—	—	mA
High-level output current, high voltage mode	Ioh_hv	Vout = 0.8 × OVDD Low Drive Medium Drive High Drive	 –5.1 –10.2 –15.3	—	—	mA
Low-level output current, low voltage mode	Iol_lv	Vout = 0.2 × OVDD Low Drive Medium Drive High Drive	 2.2 4.4 6.6	—	—	mA
Low-level output current, high voltage mode	Iol_hv	Vout = 0.2 × OVDD Low Drive Medium Drive High Drive	 5.1 10.2 15.3	—	—	mA
High-Level DC input voltage[1, 2]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1, 2]	VIL	—	0	—	0.3 × OVDD	V
Input Hysteresis	VHYS	low voltage mode high voltage mode	0.38 0.95	—	0.43 1.33	V
Schmitt trigger VT+[2, 3]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[2, 3]	VT–	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	300 63	nA
Input current (22 kΩ Pull-up)	IIN	VI = 0 VI = OVDD	—	—	202 0.06	µA
Input current (75 kΩ Pull-up)	IIN	VI = 0 VI = OVDD	—	—	61 0.06	µA
Input current (100 kΩ Pull-up)	IIN	VI = 0 VI = OVDD	—	—	47 0.06	µA
Input current (360 kΩ Pull-down)	IIN	VI = 0 VI = OVDD	—	—	0.3 5.7	µA
Keeper Circuit Resistance	—	—	—	125	—	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.3.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 16 shows the Low Voltage Differential Signaling (LVDS) DC electrical characteristics.

Table 16. LVDS DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	V_{OD}	Rload=100Ω padP, –padN	250	350	450	mV
Output High Voltage	V_{OH}		1.25	1.375	1.6	V
Output Low Voltage	V_{OL}		0.9	1.025	1.25	
Offset Voltage	V_{OS}		1.125	1.2	1.375	

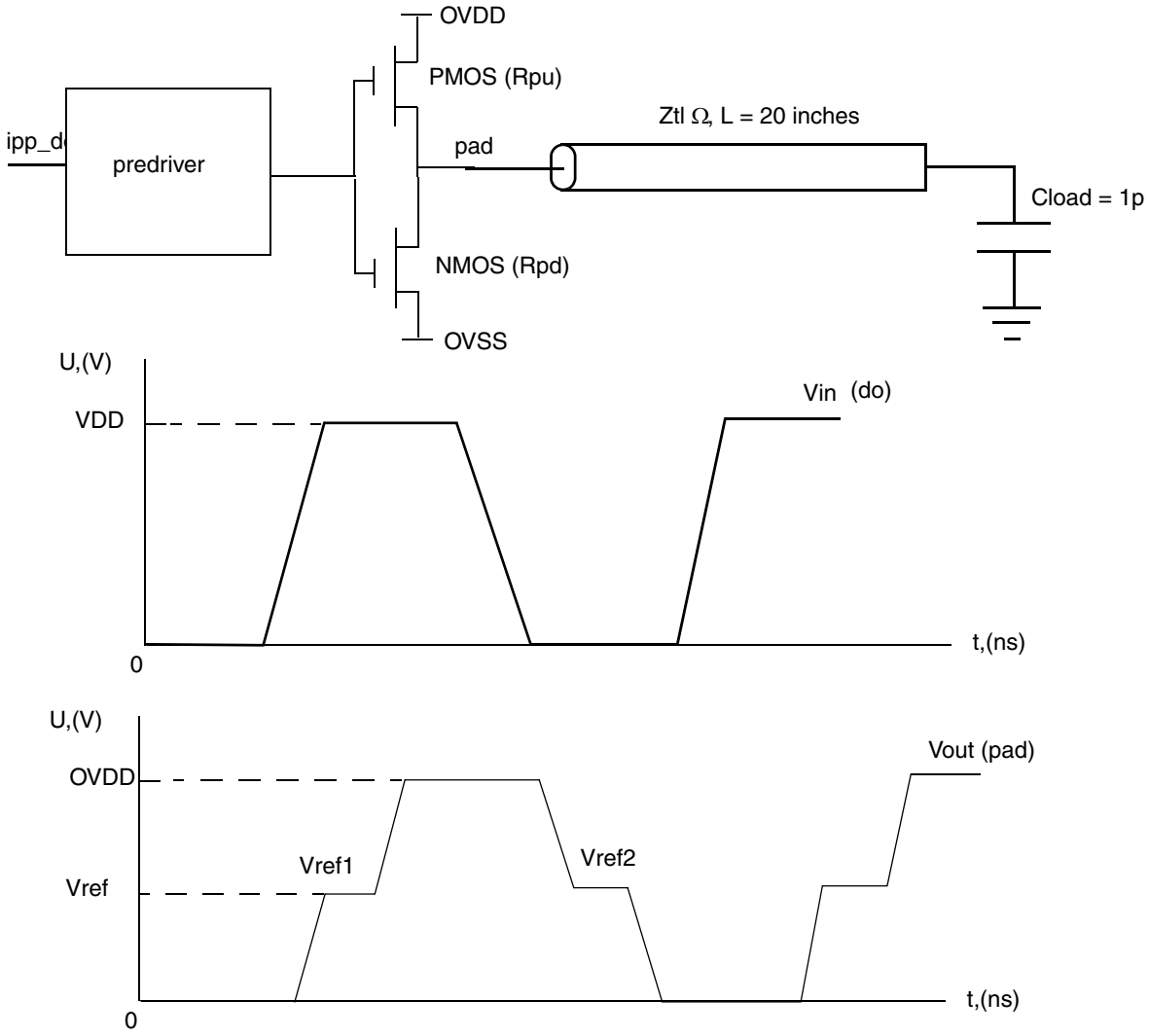
4.4 Output Buffer Impedance Characteristics

This section defines the I/O Impedance parameters of the i.MX53xA processor for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2, and DDR3 modes
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

NOTE

Output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission lime. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 4).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 4. Impedance Matching Load for Measurement

4.4.1 GPIO Output Buffer Impedance

Table 17 shows the GPIO output buffer impedance.

Table 17. GPIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875 V		
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.4.2 LPDDR2 I/O Output Buffer Impedance

The DDR2/LVDDR2 interface fully complies with JESD79-2E DDR2 JEDEC standard release April, 2008. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

4.4.3 xAUHVIO Output Buffer Impedance

Table 18 shows the UHVIO output buffer impedance.

Table 18. UHVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min		Typ		Max		Unit
			OVDD 1.95 V	OVDD 3.0 V	OVDD 1.875 V	OVDD 3.3 V	OVDD 1.65 V	OVDD 3.6 V	
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω	98 49 32	114 57 38	124 62 41	135 67 45	198 99 66	206 103 69	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω	97 49 32	118 59 40	126 63 42	154 77 51	179 89 60	217 109 72	Ω

4.4.4 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.5 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2 and DDR3 modes

- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

The load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

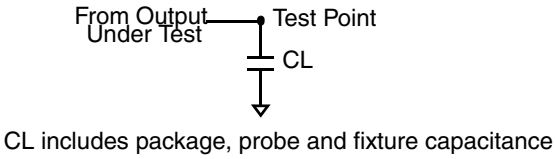


Figure 5. Load Circuit for Output

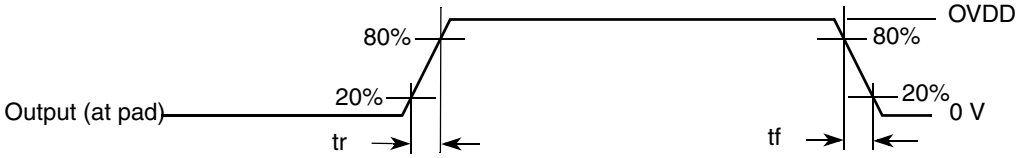


Figure 6. Output Transition Time Waveform

4.5.1 GPIO I/O AC Electrical Characteristics

AC electrical characteristics for GPIO I/O in slow and fast modes are presented in the Table 19 and Table 20, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUXC control registers.

Table 19. GPIO I/O AC Parameters Slow Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.91/1.52 3.07/2.65	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	2.22/1.81 3.81/3.42	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.88/2.42 5.43/5.02	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.94/4.50 10.55/9.70	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.5/0.65 0.32/0.37	—	—	V/ns
Output Pad Slew Rate (High Drive)[1]	tps	15 pF 35 pF	0.43/0.54 0.26/0.41	—	—	
Output Pad Slew Rate (Medium Drive)[1]	tps	15 pF 35 pF	0.34/0.41 0.18/0.2	—	—	
Output Pad Slew Rate (Low Drive)[1]	tps	15 pF 35 pF	0.20/0.22 0.09/0.1	—	—	

Table 19. GPIO I/O AC Parameters Slow Mode (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad di/dt (Max Drive)	tdit	—	—	—	30	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	23	
Output Pad di/dt (Medium drive)	tdit	—	—	—	15	
Output Pad di/dt (Low drive)	tdit	—	—	—	7	
Input Transition Times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 20. GPIO I/O AC Parameters Fast Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.45/1.24 2.76/2.54	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	1.81/1.59 3.57/3.33	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.54/2.29 5.25/5.01	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.82/4.5 10.54/9.95	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.69/0.78 0.36/0.39	—	—	V/ns
Output Pad Slew Rate (High Drive)[1]	tps	15 pF 35 pF	0.55/0.62 0.28/0.30	—	—	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15 pF 35 pF	0.39/0.44 0.19/0.20	—	—	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15 pF 35 pF	0.21/0.22 0.09/0.1	—	—	V/ns
Output Pad di/dt (Max Drive)	tdit	—	—	—	70	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	53	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	35	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	18	mA/ns
Input Transition Times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.2 LPDDR2 I/O AC Electrical Characteristics

The DDR2/LVDDR2 interface mode fully complies with JESD79-2E DDR2 JEDEC standard release April, 2008. The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 21 shows the AC parameters for LPDDR2 I/O operating in DDR2 mode.

Table 21. LPDDR2 I/O DDR2 mode AC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref+0.25	—	—	V
AC input logic low	Vil(ac)	—	—	—	Vref-0.25	V
AC differential input voltage[2]	Vid(ac)	—	0.5	—	OVDD	V
Input AC differential cross point voltage[3]	Vix(ac)	—	Vref – 0.175	—	Vref + 0.175	V
Output AC differential cross point voltage[4]	Vox(ac)	—	Vref – 0.125	—	Vref + 0.125	V
Single output slew rate	tsr	At 25 Ω to Vref	0.4	—	2	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk=266Mhz clk=400Mhz	—	—	0.2 0.1	ns

1 Note that the JEDEC SSTL_18 specification (JESD8-15a) for class II operation supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4 The typical value of Vox(ac) is expected to be about 0.5 * OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

Table 22 shows the AC parameters for LPDDR2 I/O operating in LPDDR2 mode.

Table 22. LPDDR2 I/O LPDDR2 mode AC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to OVDD/2	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	266MHz	—	—	0.6	V*ns

Table 22. LPDDR2 I/O LPDDR2 mode AC Characteristics[1] (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single output slew rate	tsr	50Ohm to Vref. 5pF load. Drive impedance= 40Ohm +-30%	1.5	—	3.5	V/ns
		50Ohm to Vref. 5pF load.Drive impedance= 60Ohm +-30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk=266MHz clk=400MHz	—	—	0.2 0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 23 shows the AC parameters for LPDDR2 I/O operating in DDR3 mode.

Table 23. LPDDR2 I/O DDR3 mode AC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	—	Vref – 0.15	—	Vref + 0.15	V
Output AC differential cross point voltage[4]	Vox(ac)	—	Vref – 0.15	—	Vref + 0.15	V
Single output slew rate	tsr	At 25 Ω to Vref	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk=266MHz clk=400MHz	—	—	0.2 0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4 The typical value of Vox(ac) is expected to be about 0.5 * OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

4.5.3 LVIO I/O AC Electrical Characteristics

AC electrical characteristics for LVIO I/O in slow and fast modes are presented in the Table 24 and Table 25, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUXC control registers.

Table 24. LVIO I/O AC Parameters in Slow Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.5.4 UHVIO I/O AC Electrical Characteristics

Table 25. LVIO I/O AC Parameters in Fast Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

Table 26 shows the AC parameters for UHVIO I/O operating in low output voltage mode. Table 27 shows the AC parameters for UHVIO I/O operating in high output voltage mode.

Table 26. AC Electrical Characteristics of UHVIO Pad (Low Output Voltage Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	1.59/1.69 3.05/3.30	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.16/2.35 4.45/4.84	
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.06/4.42 8.79/9.55	
Output Pad Slew Rate (High Drive)[1]	tps	15 pF 35 pF	0.63/0.59 0.33/0.30	—	—	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15 pF 35 pF	0.46/0.42 0.22/0.21	—	—	
Output Pad Slew Rate (Low Drive)[1]	tps	15 pF 35 pF	0.25/0.23 0.11/0.11	—	—	
Output Pad di/dt (High Drive)	tdit	—	—	—	43.6	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	32.3	
Output Pad di/dt (Low drive)	tdit	—	—	—	18.24	
Input Transition Times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 27. AC Electrical Characteristics of UHVIO Pad (High Output Voltage Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	1.72/1.92 3.46/3.70	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.38/2.56 5.07/5.25	
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.55/4.58 10.04/9.94	
Output Pad Slew Rate (High Drive)[1]	tps	15 pF 35 pF	1.05/0.94 0.52/0.49	—	—	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15 pF 35 pF	0.76/0.71 0.36/0.34	—	—	
Output Pad Slew Rate (Low Drive)[1]	tps	15 pF 35 pF	0.40/0.93 0.18/0.18	—	—	
Output Pad di/dt (High Drive)	tdit	—	—	—	82.8	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	65.6	
Output Pad di/dt (Low drive)	tdit	—	—	—	43.1	
Input Transition Times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.5.5 LVDS I/O AC Electrical Characteristics

The differential output transition time waveform is shown in Figure 7.

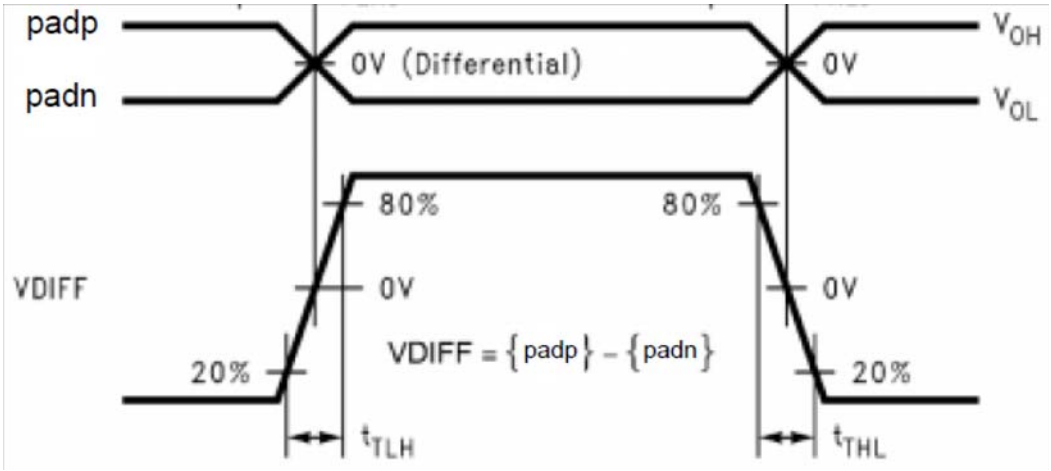


Figure 7. Differential LVDS Driver Transition Time Waveform

Table 28 shows the AC parameters for LVDS I/O.

Table 28. AC Electrical Characteristics of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		0.26	—	0.5	
Transition High to Low Time[2]	t_{THL}		0.26	—	0.5	
Operating Frequency	f	—	—	300	—	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

1 t_{SKD} = | t_{PHLD} – t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

4.6 System Modules Timing

This section contains the timing and electrical parameters for the modules in the i.MX53xA processor.

4.6.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 29 lists the timing parameters.

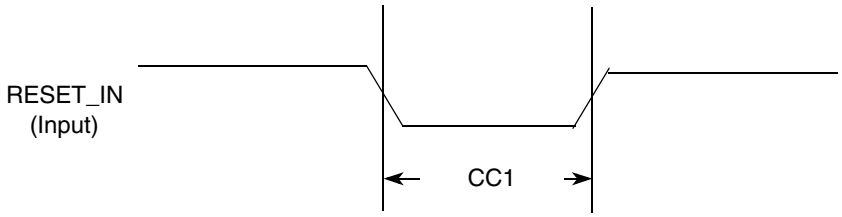


Figure 8. Reset Timing Diagram

Table 29. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of RESET_IN to be qualified as valid (input slope = 5 ns)	50	—	ns

4.6.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 30 lists the timing parameters.

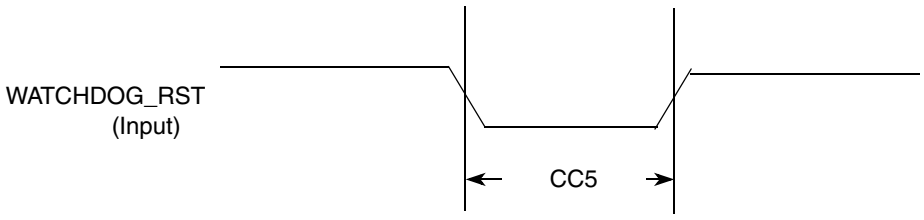


Figure 9. WATCHDOG_RST Timing Diagram

Table 30. WATCHDOG_RST Timing Parameters

ID	Parameter	Min	Max	Unit
CC5	Duration of WATCHDOG_RESET Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

4.6.3 Clock Amplifier Parameters (CKIH1, CKIH2)

The input to Clock Amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required.

Table 31 shows the electrical parameters of CAMP.

Table 31. CAMP Electrical Parameters (CKIH1, CKIH2)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)[1]	NVCC_CKIH – 0.25	—	NVCC_CKIH	V
Sinusoidal input amplitude[2]	0.4	—	VDD	Vp-p
Output duty cycle	45	50	55	%

1 NVCC_CKIH is the supply voltage of CAMP.

2 Minimum value of the sinusoidal input will be determined during characterization.

4.6.4 DPLL Electrical Parameters

Table 32 shows the electrical parameters of digital phase-locked loop (DPLL).

Table 32. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output Duty Cycle	—	48.5	50	51.5	%

Table 32. DPLL Electrical Parameters (continued)

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Frequency lock time[4] (FOL mode or non-integer MF)	—	—	—	398	T_{dpdref}
Phase lock time	—	—	—	100	µs
Frequency jitter[5] (peak value)	—	—	0.02	0.04	T_{dck}
Phase jitter (peak value)	FPL mode, integer and fractional MF	—	2.0	3.5	ns
Power dissipation	f_{dck} = 300 MHz @ avdd = 1.8 V, dvdd = 1.2 V f_{dck} = 650 MHz @ avdd = 1.8 V, dvdd = 1.2 V	—	—	0.65 (avdd) 0.92 (dvdd) 1.98 (avdd) 1.8 (dvdd)	mW

1 Device input range cannot exceed the electrical specifications of the CAMP, see Table 31.

2 The values specified here are internal to DPLL. Inside the DPLL, a “1” is added to the value specified by the user. Therefore, the user has to enter a value “1” less than the desired value at the inputs of DPLL for PDF and MFD.

3 The maximum total multiplication factor (MFI + MFN/MFD) allowed is 15. Therefore, if the MFI value is 15, MFN value must be zero.

4 T_{dpdref} is the time period of the reference clock after predivider. According to the specification, the maximum lock time in FOL mode is 398 cycles of divided reference clock when DPLL starts after full reset.

5 Tdck is the time period of the output clock, dpdck_2.

4.6.5 NAND Flash Controller (NFC) Parameters

This section provides the relative timing requirements among various signals of NFC at the module level, in each operational mode.

Timing parameters in Figure 10, Figure 11, Figure 12, Figure 13, Figure 15, and Table 34 show the default NFC mode (asymmetric mode) using two Flash clock cycles per one access of RE_B and WE_B.

Timing parameters in Figure 10, Figure 11, Figure 12, Figure 14, Figure 15, and Table 34 show symmetric NFC mode using one Flash clock cycle per one access of RE_B and WE_B.

With reference to the timing diagrams, a high is defined as 80% of signal value and low is defined as 20% of signal value. All parameters are given in nanoseconds. The BGA contact load used in calculations is 20 pF (except for NF16 - 40 pF) and there is maximum drive strength on all contacts.

All timing parameters are a function of T, which is the period of the flash_clk clock (“enfc_clk” at system level). This clock frequency can be controlled by the user, configuring CCM (SoC clock controller). The clock is derived from emi_slow_clk after single divider.

Table 33 demonstrates several examples of clock frequency settings.

Table 33. NFC Clock Settings Examples

emi_slow_clk (MHz)	nfc_podf (Division Factor)	enfc_clk (MHz)	T-Clock Period (ns)
100 (Boot mode)	7[1]	14.29	70
	3[2]	33.33	30

Table 33. NFC Clock Settings Examples (continued)

emi_slow_clk (MHz)	nfc_podf (Division Factor)	enfc_clk (MHz)	T-Clock Period (ns)
133	4	33.33	30
	3	44.33[3]	22.5
	2	66[3]	15

1 Boot value NFC_FREQ_SEL Fuse High (burned)

2 Boot value NFC_FREQ_SEL Fuse Low

3 For RBB_MODE=1, using NANDF_RB0 signal for ready/busy indication. This mode require setting the delay line. See the Reference Manual for details.

NOTE

A potential limitation for minimum clock frequency may exist for some devices. When the clock frequency is too low, the data bus capturing might occur after the specified t_{rhoh} (RE_B high to output hold) period. Setting the clock frequency above 25.6 MHz (that is, T = 39 ns) guaranties a proper operation for devices having t_{rhoh} > 15 ns. It is also recommended that the NFC_FREQ_SEL Fuse be set accordingly to initiate the boot with 33.33 MHz clock.

Lower frequency operation can be supported for most available devices in the market, relying on data lines Bus-Keeper logic. This depends on device behavior on the data bus in the time interval between data output valid to data output high-Z state. In NAND device parameters this period is marked between t_{rhoh} and t_{rhz} (RE_B high to output high-Z). In most devices, the data transition from valid value to high-Z occurs without going through other states. Setting the data bus pads to Bus-Keeper mode in the IOMUXC registers, keeps the data bus valid internally after the specified hold time, allowing proper capturing with slower clock.

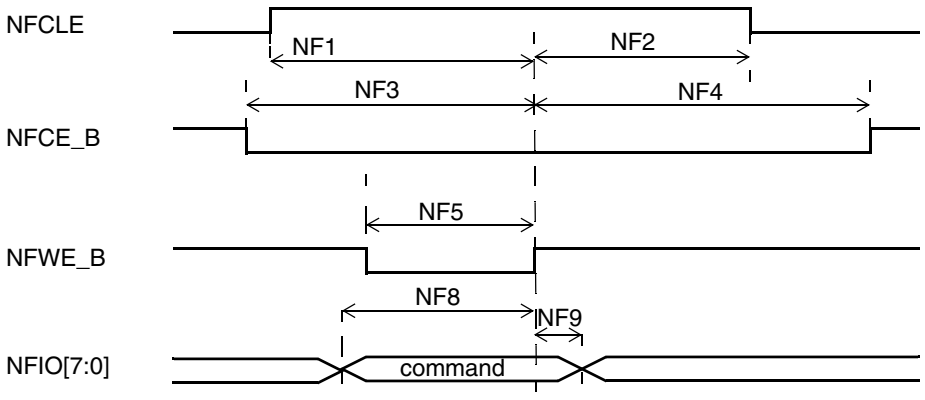


Figure 10. Command Latch Cycle Timing

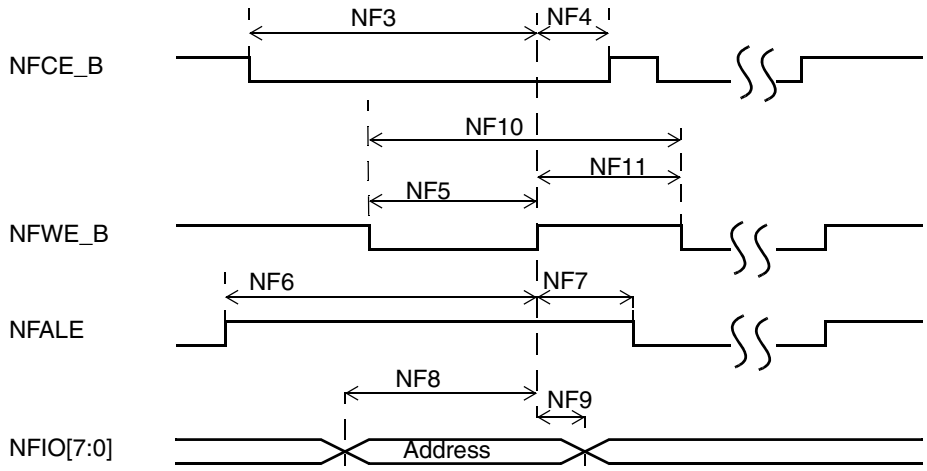


Figure 11. Address Latch Cycle Timing

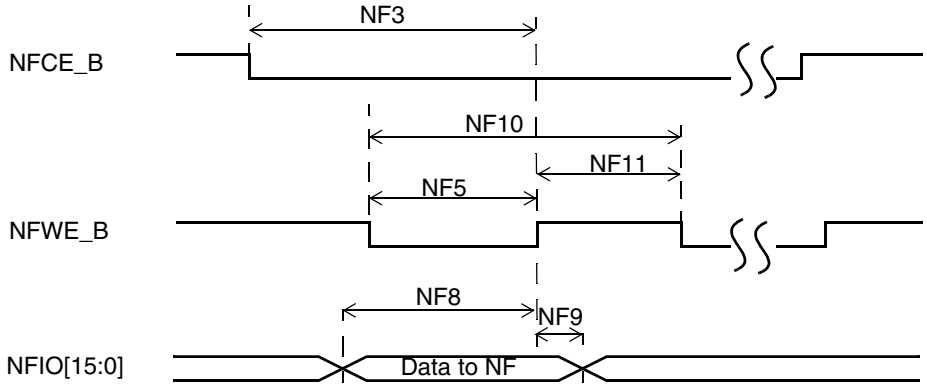


Figure 12. Write Data Latch Timing

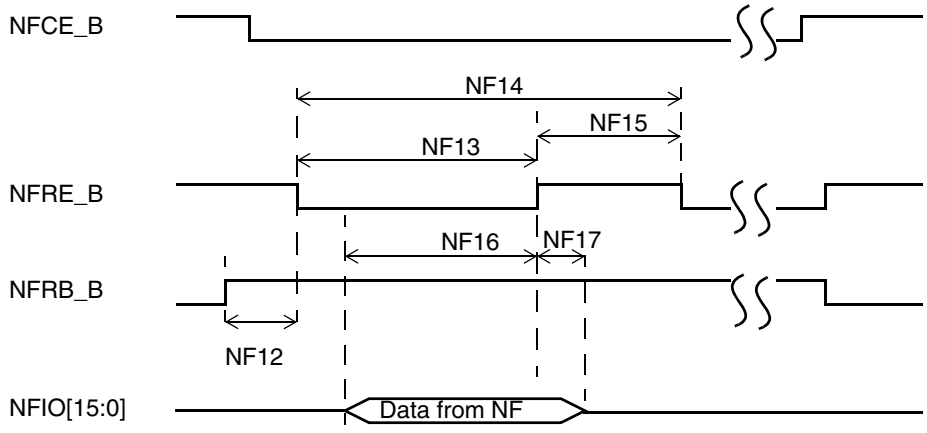


Figure 13. Read Data Latch Timing, Asymmetric Mode

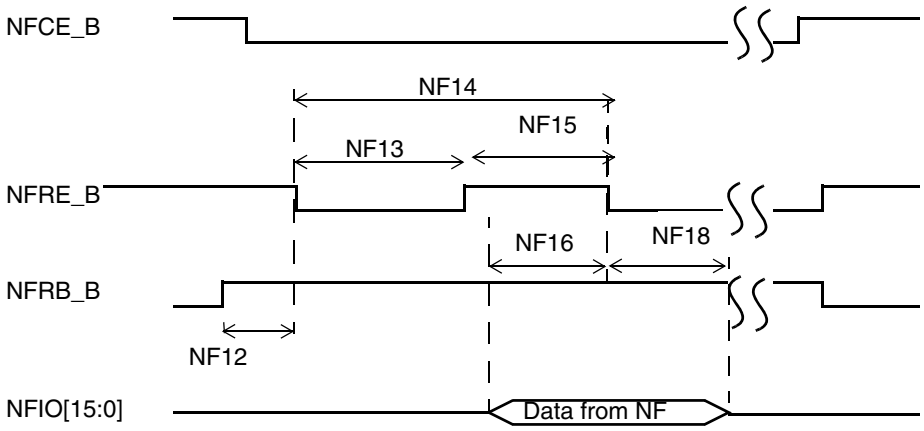


Figure 14. Read Data Latch Timing, Symmetric Mode

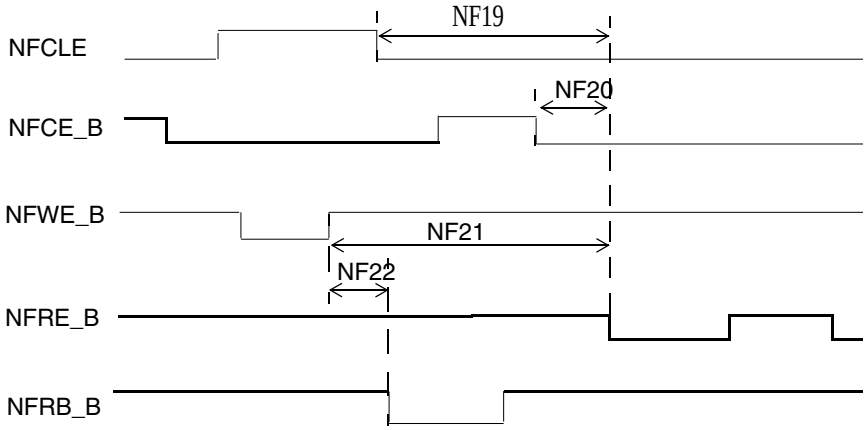


Figure 15. Other Timing Parameters

Table 34. NFC—Timing Characteristics

ID	Parameter	Symbol	Asymmetric Mode Min	Symmetric Mode Min	Max
NF1	NFCLE setup Time	t_{CLS}	2T + 0.1	2T + 0.1	—
NF2	NFCLE Hold Time	t_{CLH}	T – 4.45	T – 4.45	—
NF3	NFCE_B Setup Time	t_{CS}	3T + 0.95	3T+0.95	—
NF4	NFCE_B Hold Time	t_{CH}	3T – 5.55	3T – 5.55	—
NF5	NFWE_B Pulse Width	t_{WP}	T – 1.4	0.5T – 1.4	—
NF6	NFALE Setup Time	t_{ALS}	2T + 0.1	2T + 0.1	—
NF7	NFALE Hold Time	t_{ALH}	T – 4.45	T – 4.45	—
NF8	Data Setup Time	t_{DS}	T – 0.9	0.5T – 0.9	—
NF9	Data Hold Time	t_{DH}	T – 5.55	0.5T – 5.55	—
NF10	Write Cycle Time	t_{WC}	2T	T	—
NF11	NFWE_B Hold Time	t_{WH}	T – 1.15	0.5T – 1.15	—
NF12	Ready to NFRE_B Low	t_{RR}	9T + 8.9	9T + 8.9	—
NF13	NFRE_B Pulse Width	t_{RP}	1.5T	0.5T	—
NF14	READ Cycle Time	t_{RC}	2T	T	—
NF15	NFRE_B High Hold Time	t_{REH}	0.5T – 1.15	0.5T – 1.15	—
NF16[1]	Data Setup on READ	t_{DSR}	$11.2 + 0.5T - Tdl^2$	$11.2 - Tdl^2$	—
NF17[3]	Data Hold on READ	t_{DHR}	0	—	$2T_{aclk} + T$
NF18[4]	Data Hold on READ	t_{DHR}	—	$Tdl^2 - 11.2$	$2T_{aclk} + T$
NF19	CLE to RE delay	t_{CLR}	13T + 1.5	13T + 1.5	—
NF20	CE to RE delay	t_{CRE}	T – 3.45	T – 3.45	T + 0.3
NF21	WE high to RE low	t_{WHR}	14T – 5.45	14T – 5.45	—
NF22	WE high to busy	t_{WB}	—	—	6T

1 t_{DSR} is calculated by the following formula:

Asymmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} + {}^1/_2T - Tdl^2$

Symmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} - Tdl^2$

$t_{REpd} + t_{Dpd}$ = 11.2 ns (including clock skew)

where t_{REpd} is RE propogation delay in the chip including I/O pad delay, and t_{Dpd} is Data propogation delay from I/O pad to EXTMC including I/O pad delay.

t_{DSR} can be used to determine t_{REA} max parameter with the following formula: $t_{REA} = 1.5T - t_{DSR}$.

2 Tdl is composed of 4 delay-line units each generates an equal delay with min 1.25 ns and max 1 aclk period (T_{aclk}). Default is 1/4 aclk period for each delay-line unit, so all 4 delay lines together generates a total of 1 aclk period. T_{aclk} is “emi_slow_clk” of the system, which default value is 7.5 ns (133 MHz).

3 NF17 is defined only in asymmetric operation mode.

NF17 max value is equivalent to max t_{RHZ} value that can be used with NFC.

T_{aclk} is “emi_slow_clk” of the system.

4 NF18 is defined only in Symmetric operation mode.
t_{DHR} (MIN) is calculated by the following formula: $Tdl^2 - (t_{REpd} + t_{Dpd})$
where t_{REpd} is RE propogation delay in the chip including I/O pad delay, and t_{Dpd} is Data propogation delay from I/O pad to EXTMC including I/O pad delay.
NF18 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4.6.6 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.6.6.1 EIM Signal Cross Reference

Table 35 is a guide intended to help the user identify signals in the External Interface Module Chapter of the Reference Manual which are identical to those mentioned in this data sheet.

Table 35. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA
ADDR	EIM_A[25:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.6.6.2 EIM Interface Pads Allocation

EIM supports16-bit and 8-bit devices operating in address/data separate or multiplexed modes. In some of the modes the EIM and the NAND FLASH have shared data bus. Table 37 provides EIM interface pads allocation in different modes.

Table 36. EIM Internal Module Multiplexing

Setup	Non Multiplexed Address/Data Mode		Multiplexed Address/Data mode
	8 Bit	16 Bit	16 Bit
	MUM = 0, DSZ = 111	MUM = 0, DSZ = 010	MUM = 1, DSZ = 001
A[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]
A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[25:16]
D[7:0], EIM_EB0	—	—	EIM_DA[7:0]
D[15:8], EIM_EB1	—	—	EIM_DA[15:8]
D[23:16], EIM_EB2	—	EIM_D[23:16]	—
D[31:24], EIM_EB3	EIM_D[31:24]	EIM_D[31:24]	—

Table 37. Revision 2.0 EIM Internal Module Multiplexing

Setup	Non Multiplexed Address/Data Mode						Multiplexed Address/Data mode	
	8 Bit			16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 111	MUM = 0, DSZ = 111	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
A[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]
A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[24:16][1]	EIM_A[25:16]	NANDF_D[8:0][1]
D[7:0], EIM_EB0	NANDF_D[7:0][2]	—	—	NANDF_D[7:0][2]	—	NANDF_D[7:0]	EIM_DA[7:0]	EIM_DA[7:0]
D[15:8], EIM_EB1	—	NANDF_D[15:8][3]	—	NANDF_D[15:8][3]	—	NANDF_D[15:8]	EIM_DA[15:8]	EIM_DA[15:8]
D[23:16], EIM_EB2	—	—	—	—	EIM_D[23:16]	EIM_D[23:16]	—	NANDF_D[7:0]
D[31:24], EIM_EB3	—	—	EIM_D[31:24]	—	EIM_D[31:24]	EIM_D[31:24]	—	NANDF_D[15:8]

1 For 32-bit mode, the address range is A[24:0], due to address space allocation in memory map.

2 NANDF_D[7:0] multiplexed on ALT3 mode of PATA_DATA[7:0]

3 NANDF_D[15:8] multiplexed on ALT3 mode of PATA_DATA[15:8]

4.6.6.3 General EIM Timing-Synchronous Mode

Figure 16, Figure 17, and Table 38 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

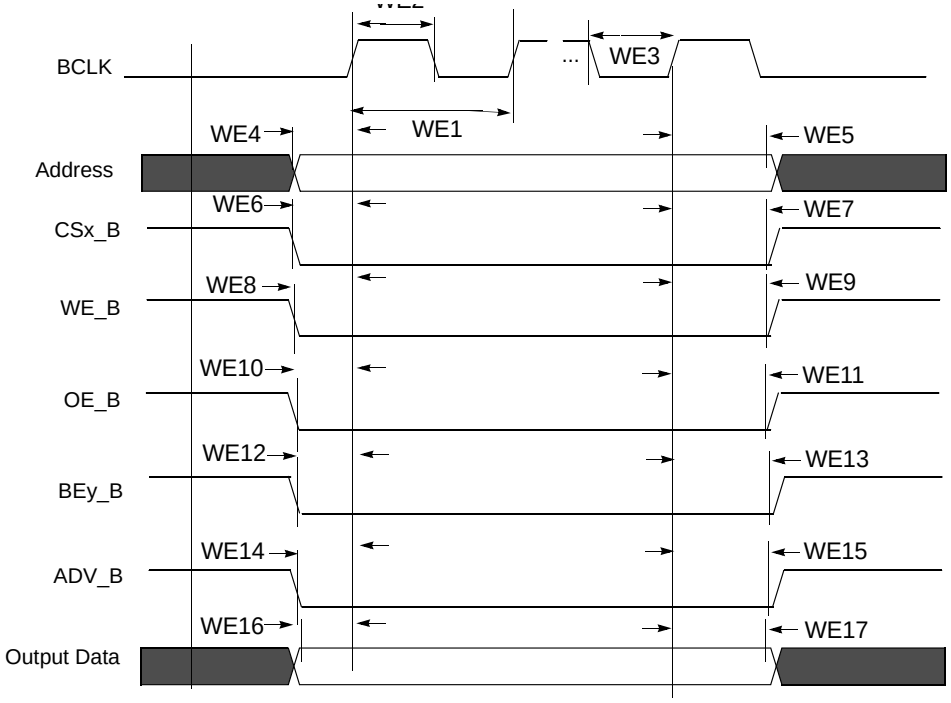


Figure 16. EIM Outputs Timing Diagram

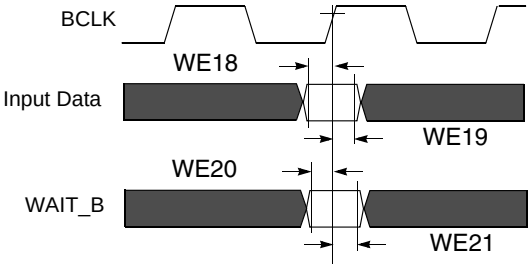


Figure 17. EIM Inputs Timing Diagram

Table 38. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	BCLK Cycle time[2]	t		2*t		3*t		4*t	
WE2	BCLK Low Level Width	0.4*t		0.8*t		1.2*t		1.6*t	

Table 38. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE3	BCLK High Level Width	0.4*t		0.8*t		1.2*t		1.6*t	
WE4	Clock rise to address valid[3]	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE5	Clock rise to address invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE6	Clock rise to CSx_B valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE7	Clock rise to CSx_B invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE8	Clock rise to WE_B Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE9	Clock rise to WE_B Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE10	Clock rise to OE_B Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE11	Clock rise to OE_B Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE12	Clock rise to BEy_B Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE13	Clock rise to BEy_B Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE14	Clock rise to ADV_B Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE15	Clock rise to ADV_B Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE16	Clock rise to Output Data Valid	-0.5*t-1.25	-0.5*t+1.75	-t-1.25	-t+1.75	-1.5*t-1.25	-1.5*t +1.75	-2*t-1.25	-2*t+1.75
WE17	Clock rise to Output Data Invalid	0.5*t-1.25	0.5*t+1.75	t-1.25	t+1.75	1.5*t-1.25	1.5*t +1.75	2*t-1.25	2*t+1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

1 t is the maximal EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed BCLK frequency is 104 MHz. As a result, if BCD = 0, axi_clk must be ≤ 104 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 104 MHz, other busses are impacted which are clocked from this source. See the CCM chapter of the i.MX53 Reference Manual for a detailed clock tree description.

2 BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

3 For signal measurements “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

4.6.6.4 Examples of EIM Synchronous Accesses

Figure 18 to Figure 21 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

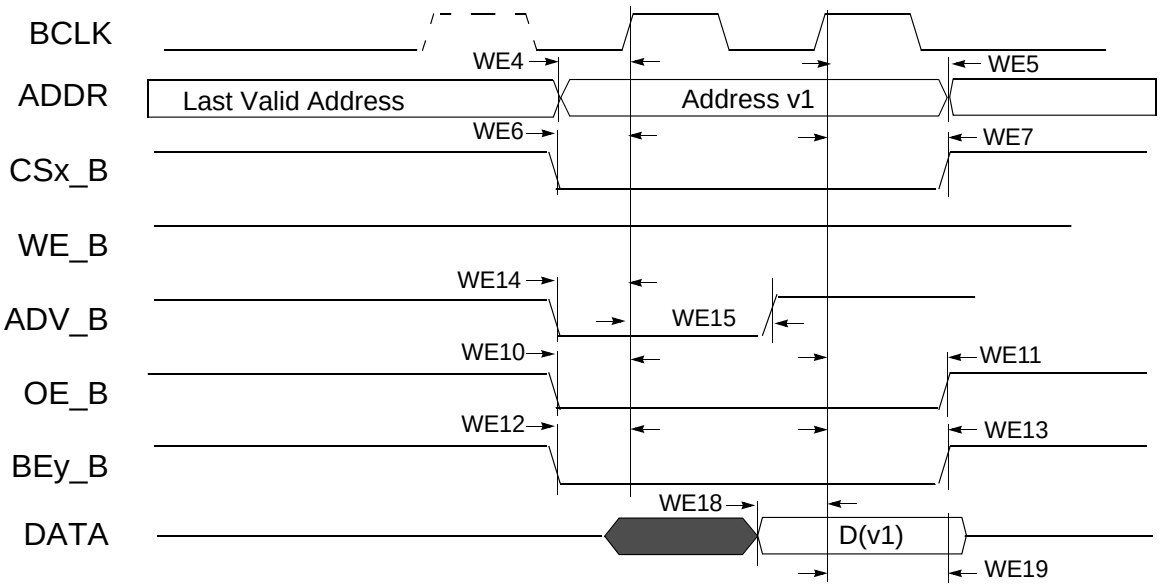


Figure 18. Synchronous Memory Read Access, WSC=1

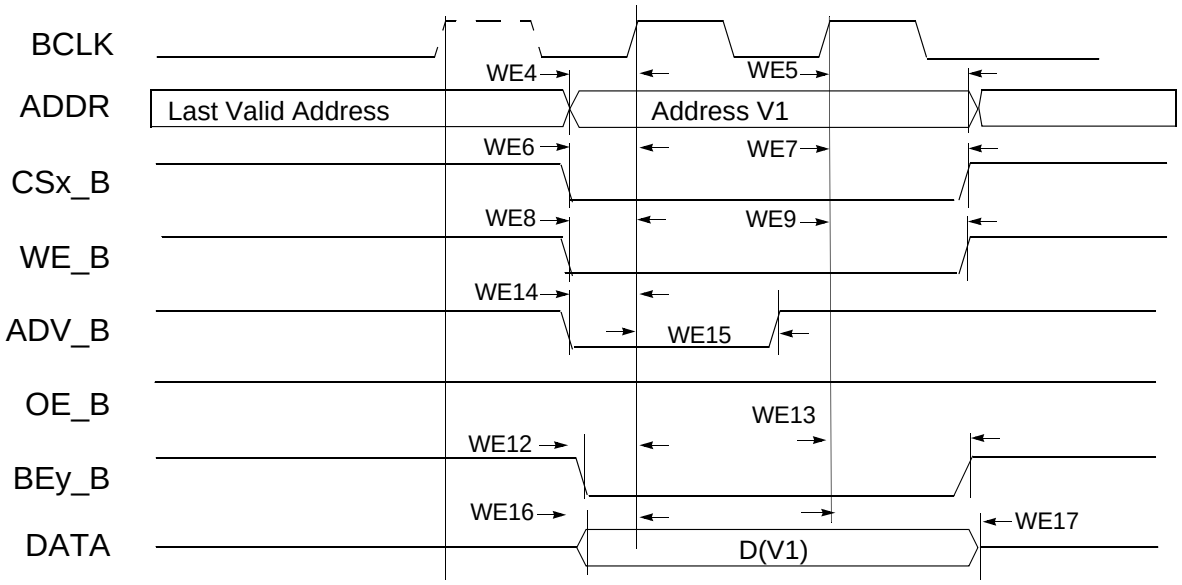


Figure 19. Synchronous Memory, Write Access, WSC=1, WBEA=1 and WADVN=0

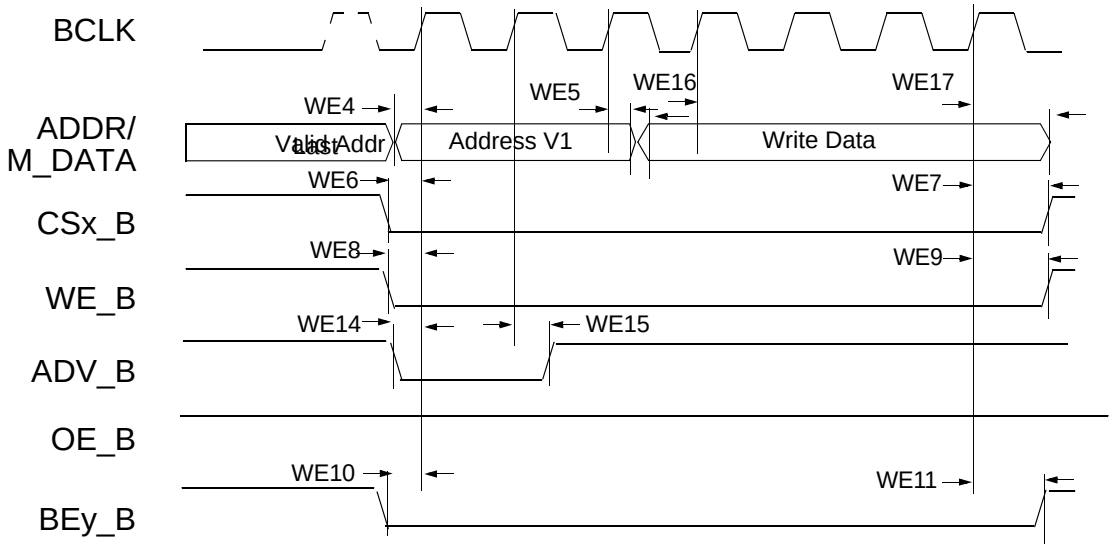


Figure 20. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=1, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

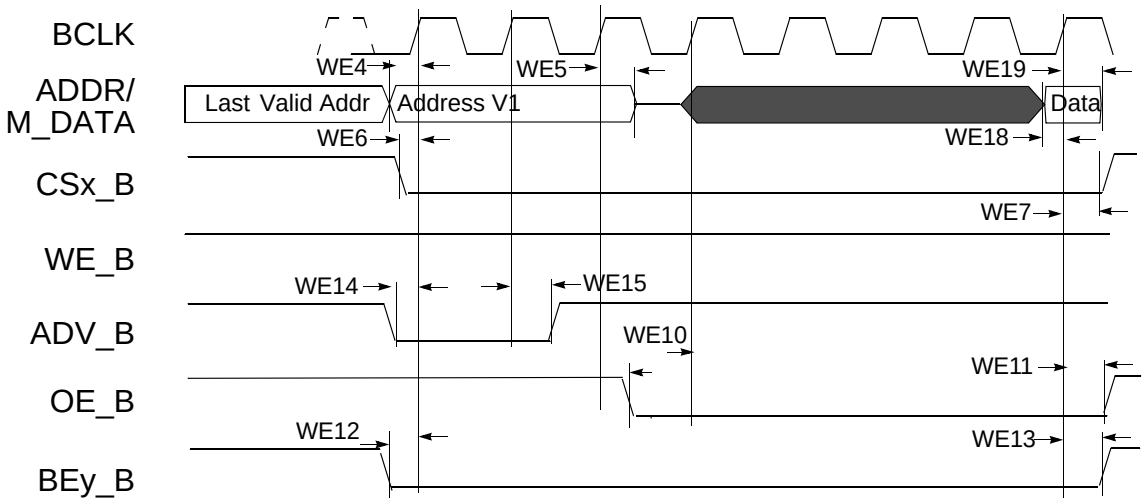


Figure 21. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=2

4.6.6.5 General EIM Timing-Asynchronous Mode

Figure 22 through Figure 26, and Table 39 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 22 through Figure 25 as RWSC, OEN & CSN is configured differently. See i.MX53xA RM for the EIM programming model.

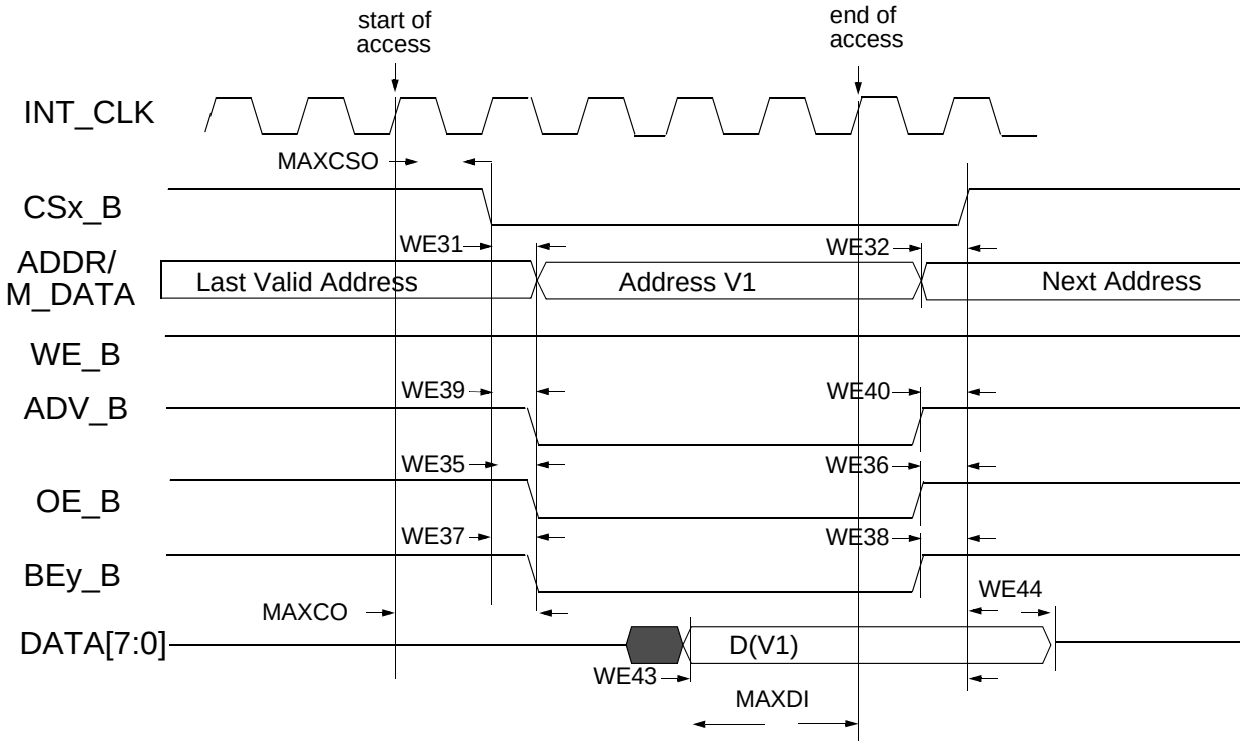


Figure 22. Asynchronous Memory Read Access (RWSC = 5, OEN=CSN=0)

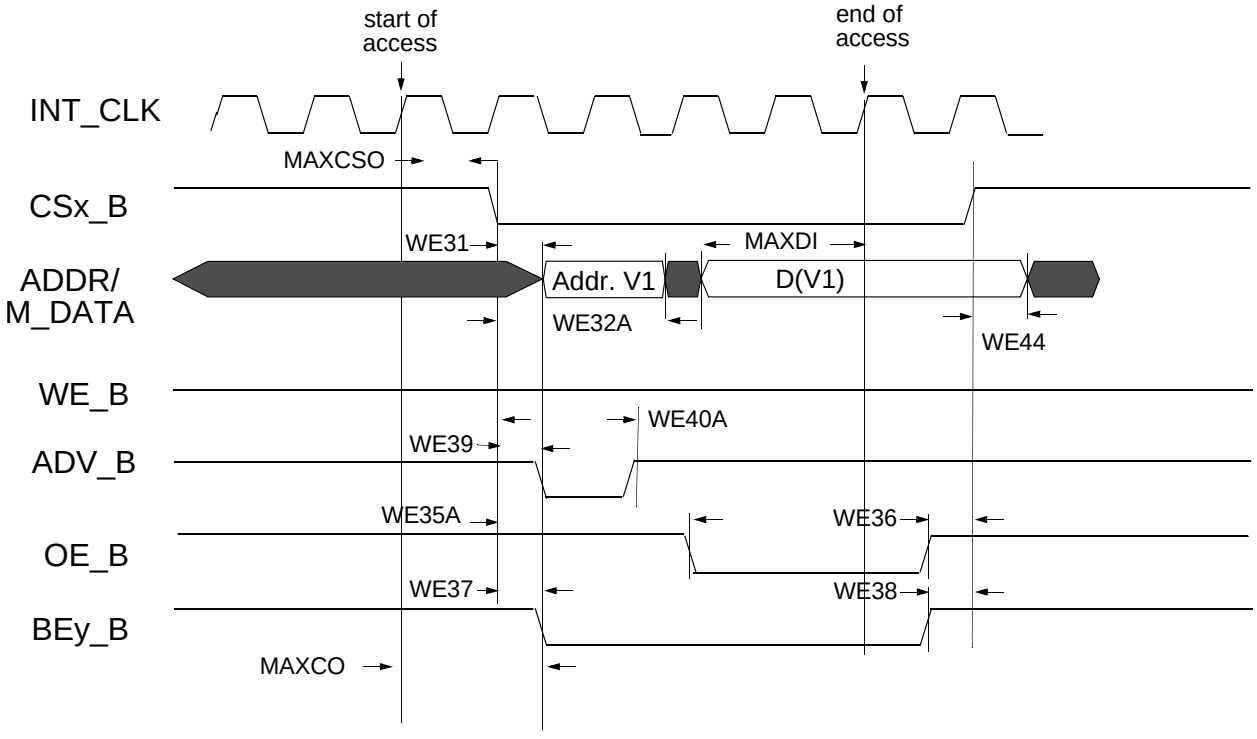


Figure 23. Asynchronous A/D Muxed Read Access (RWSC = 5, OEN=CSN=0)

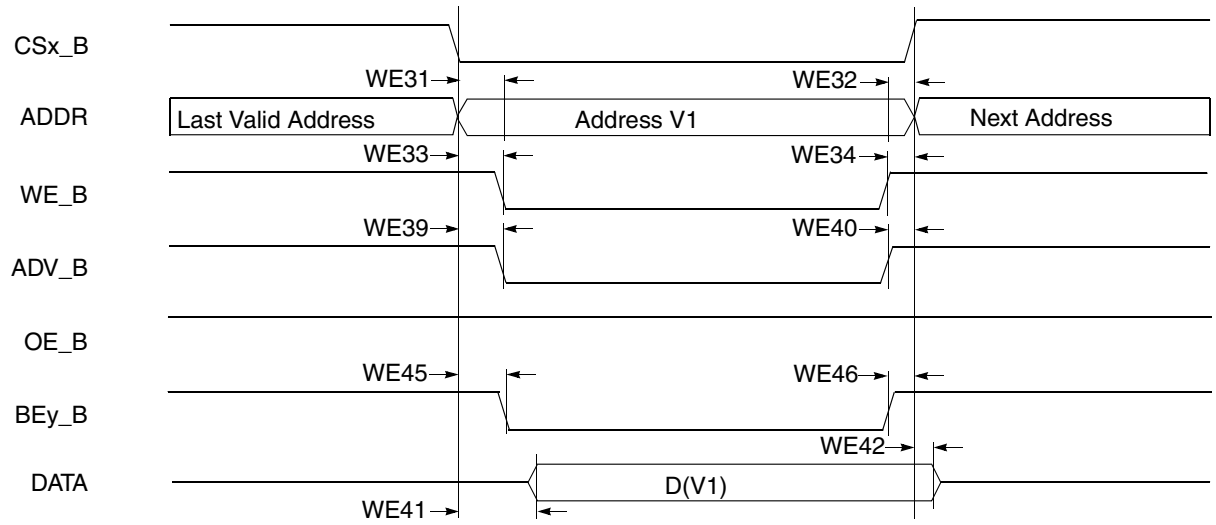


Figure 24. Asynchronous Memory Write Access (RWSC = 5, OEN=CSN=0)

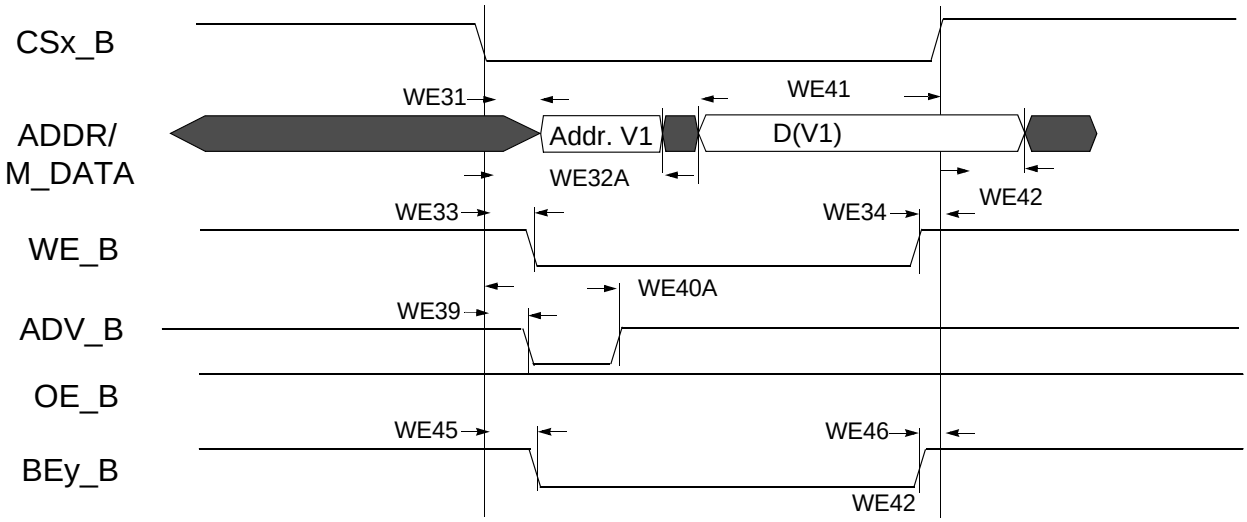


Figure 25. Asynchronous A/D Muxed Write Access (RWSC = 5, OEN=CSN=0)

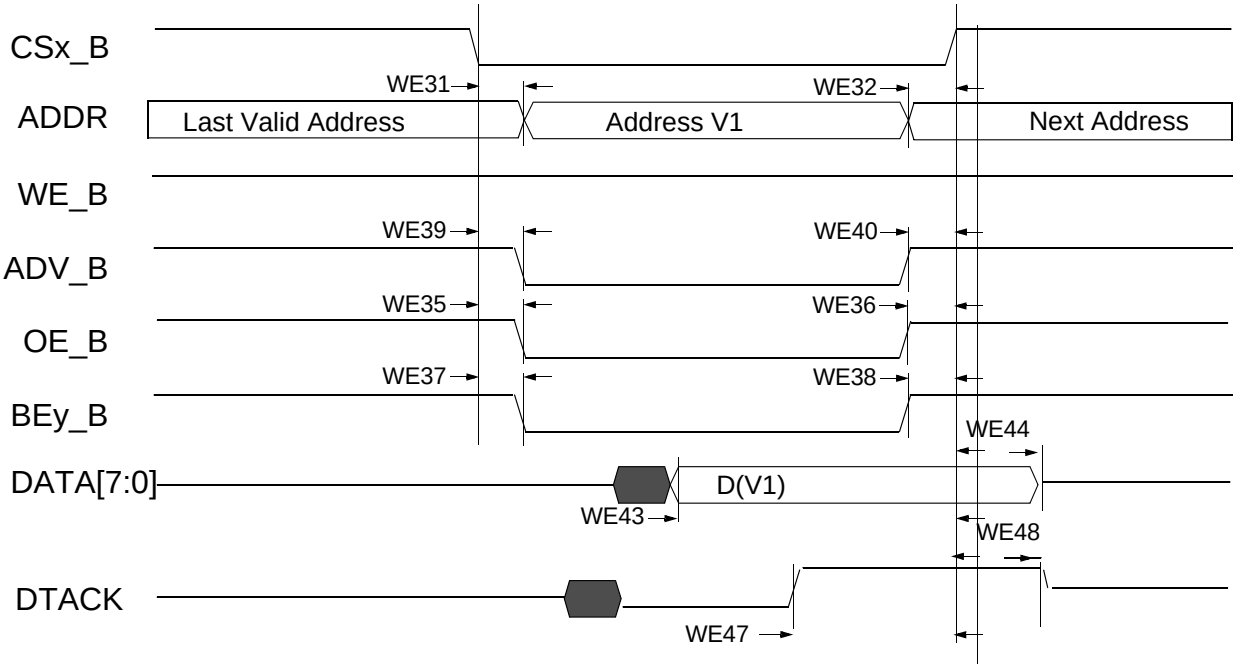


Figure 26. DTACK Read Access(DAP=0)

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 Mhz is supported by SOC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[3]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[4]	—	3 - CSN	ns
WE32A(muxed A/D	CSx_B valid to Address Invalid	t[5] + WE4 - WE7 + (ADVN + ADVA + 1 - CSA[3])	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - CSA)	—	3 + (WEA - CSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - CSN)	—	3 - (WEN_CSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - CSA)	—	3 + (OEA - CSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - CSA)	-3 + (OEA + RADVN+RADVA +ADH+1-CSA)	3 + (OEA + RADVN+RADVA+ADH+1-CSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - CSN)	—	3 - (OEN - CSN)	ns

Table 39. EIM Asynchronous Timing Parameters Table (continued)Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 Mhz is supported by SOC)	Unit
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - CSA)	—	3 + (RBEA[6] - CSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - CSN)	—	3 - (RBEN[7]- CSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCSO	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns

Table 39. EIM Asynchronous Timing Parameters Table (continued)Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 Mhz is supported by SOC)	Unit
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization		—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 Parameters WE4... WE21 value see column BCD = 0 in Table 38

2 All config. parameters (CSA,CSN,WBEA,WBEN,ADVA,ADVN,OEN,OEA,RBEA & RBEN) are in cycle units.

3 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

4 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

5 t is axi_clk cycle time.

6 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

7 BE Negation. This bit field determines when BE signal is negated during read cycles.

4.6.7 DDR SDRAM Specific Parameters (DDR2/LVDDR2, LPDDR2 and DDR3)

The DDR2/LVDDR2 interface fully complies with JESD79-2E – DDR2 JEDEC release April, 2008, supporting DDR2-800 and LVDDR2-800.

The DDR3 interface fully complies with JESD79-3D – DDR3 JEDEC release April 2008 supporting DDR3-800.

The LPDDR2 interface fully complies with JESD209-2B, supporting LPDDR2-800.

Figure 27 shows the basic timing parameters.

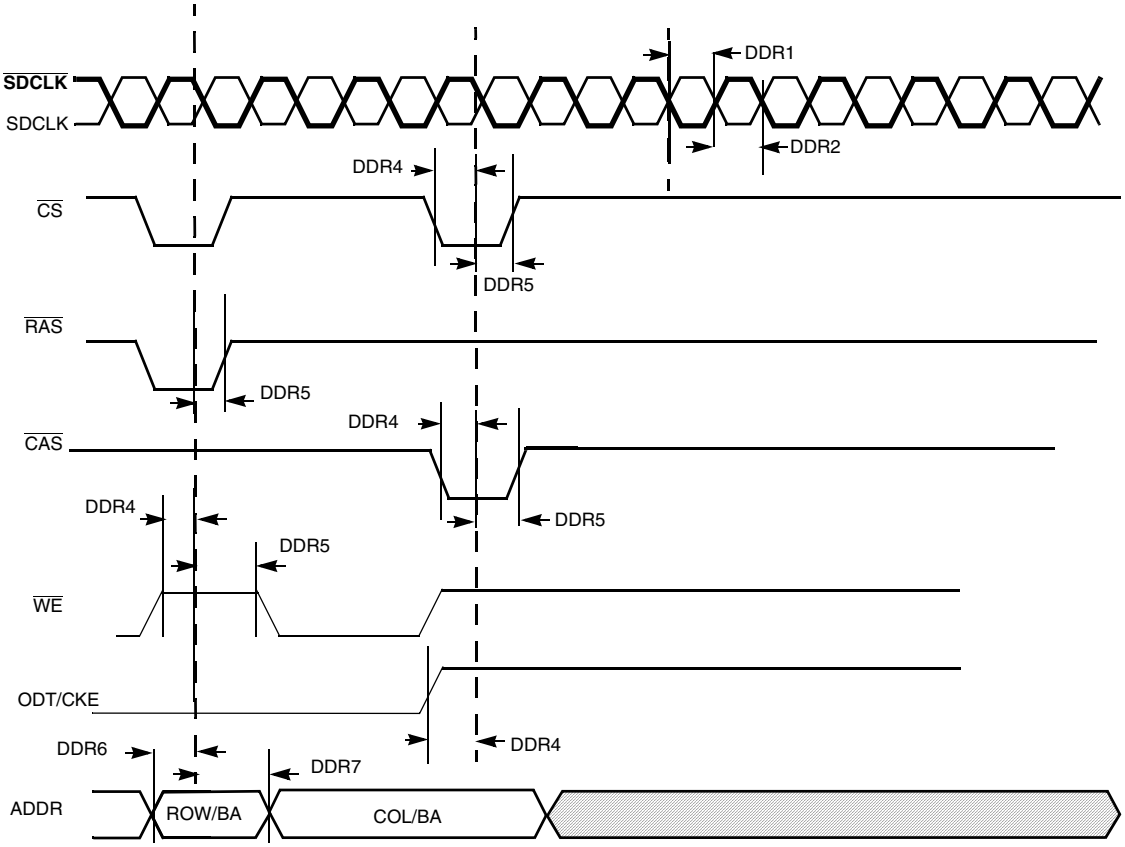


Figure 27. DDR SDRAM Basic Timing Parameters

Figure 28 shows the write timing parameters.

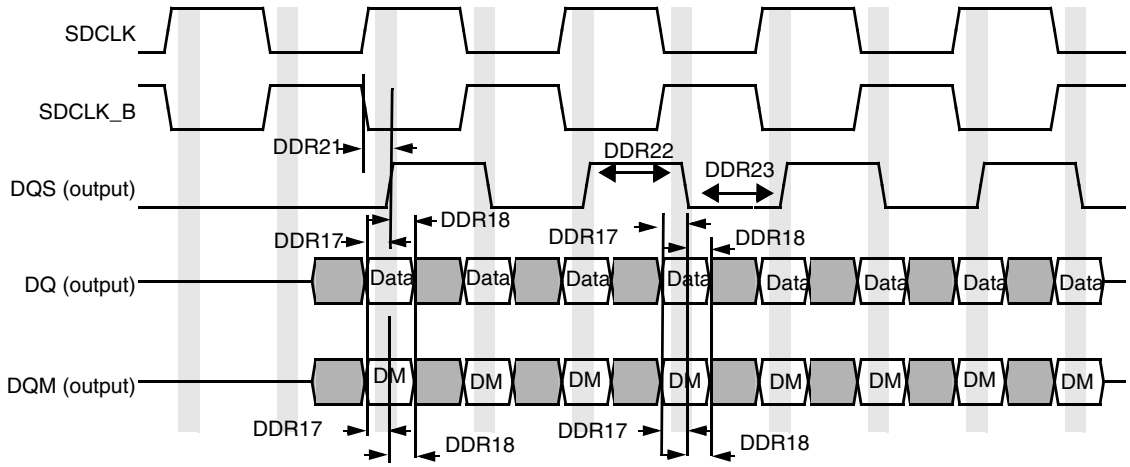


Figure 28. DDR SDRAM Write Cycle

NOTE

To receive the reported setup/hold values, write calibration should be perform to locate the DQS in the middle of DQ window.

Figure 29 shows the read timing parameters.

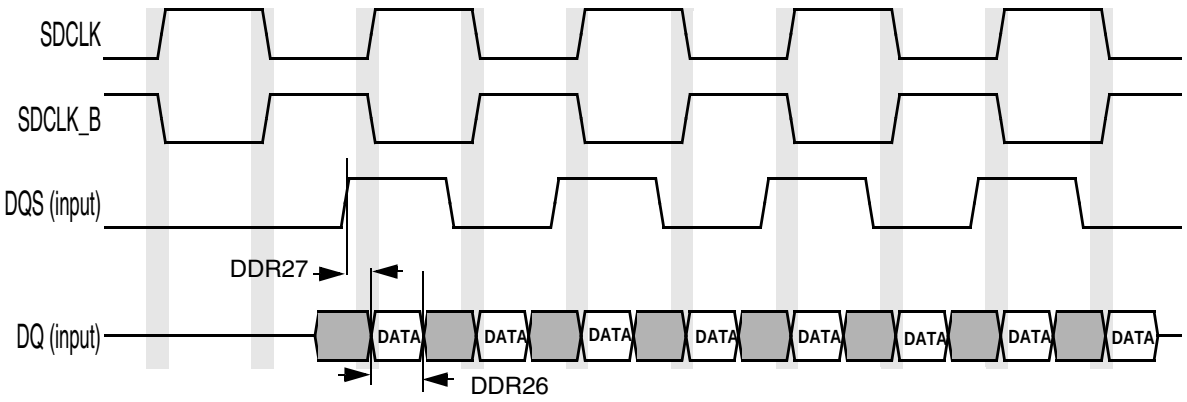


Figure 29. DDR SDRAM DQ vs. DQS and SDCLK Read Cycle

4.7 External Peripheral Interfaces Parameters

The following subsections provide information on external peripheral interfaces.

4.7.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.7.2 CSPI and ECSPI Timing Parameters

This section describes the timing parameters of the CSPI and ECSPI blocks. The CSPI and ECSPI have separate timing parameters for master and slave modes. The nomenclature used with the CSPI / ECSPI modules and the respective routing of these signals is shown in Table 40.

Table 40. CSPI Nomenclature and Routing

Block Instance	I/O Access
ECSPI-1	GPIO, KPP, DISP0_DAT, CSI0_DAT and EIM_D through IOMUXC
ECSPI-2	DISP0_DAT, CSI0_DAT and EIM through IOMUXC
CSPI	DISP0_DAT, EIM_A/D, SD1 and SD2 through IOMUXC

4.7.2.1 CSPI Master Mode Timing

Figure 30 depicts the timing of CSPI in master mode. Table 41 lists the CSPI master mode timing characteristics.

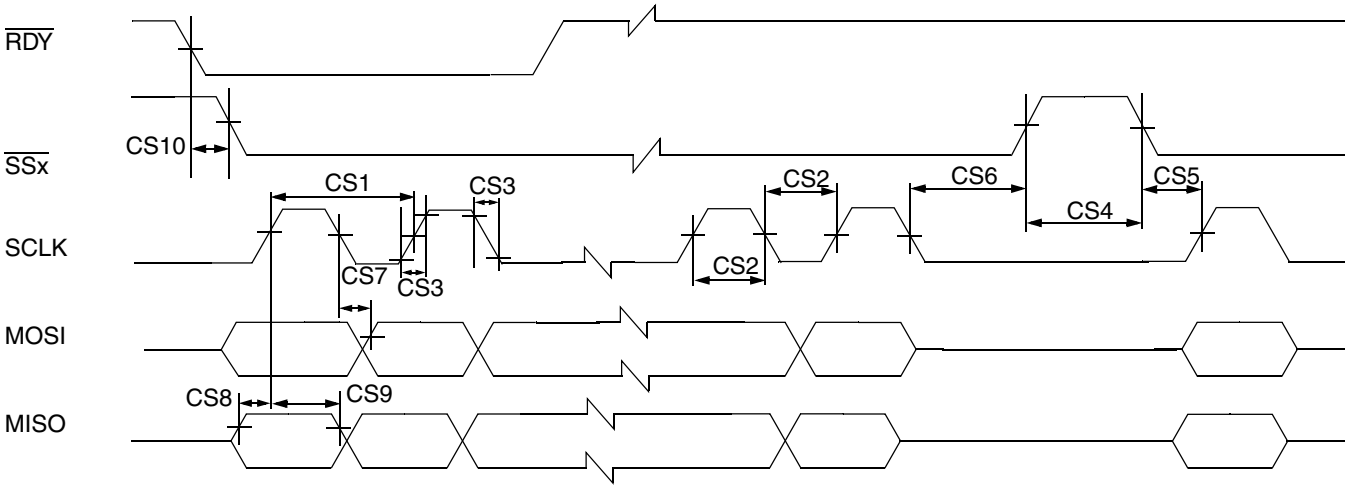


Figure 30. CSPI/ECSPI Master Mode Timing Diagram

Table 41. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns
CS5	SSx Lead Time (Slave Select setup time)	t_{SCS}	26	—	ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}	26	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	–1	21	ns
CS8	MISO Setup Time	t_{Smiso}	5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	5	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.5, “I/O AC Parameters”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.2.2 CSPI Slave Mode Timing

Figure 31 depicts the timing of CSPI in slave mode. Table 42 lists the CSPI slave mode timing characteristics.

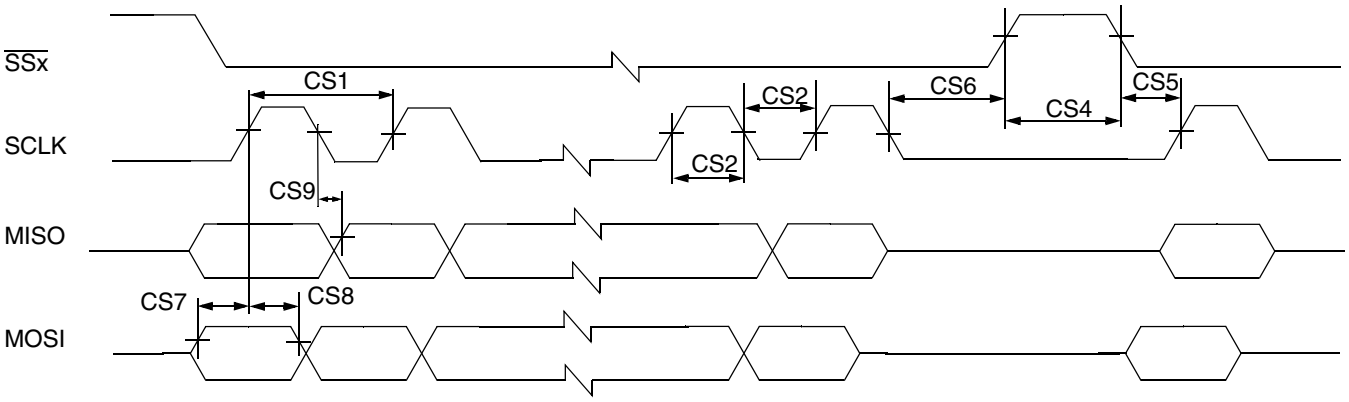


Figure 31. CSPI/ECSPI Slave Mode Timing Diagram

Table 42. CSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	100	—	ns
CS2	SCLK High or Low Time	t_{SW}		—	ns
CS4	SSx pulse width	t_{CSLH}		—	ns
CS5	SSx Lead Time (SS setup time)	t_{SCS}		—	ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}		—	ns
CS7	MOSI Setup Time	t_{Smosi}		—	ns
CS8	MOSI Hold Time	t_{Hmosi}		—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	0		ns

4.7.2.3 ECSPI Master Mode Timing

Figure 30 depicts the timing of ECSPI in master mode. Table 43 lists the ECSPI master mode timing characteristics.

Table 43. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	30 15	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	14 7	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns

Table 43. ECSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-0.5	2.5	ns
CS8	MISO Setup Time	t_{Smiso}	8.5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

[1] See specific I/O AC parameters Section 4.5, “I/O AC Parameters”

[2] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.2.4 ECSPI Slave Mode Timing

Figure 31 depicts the timing of ECSPI in slave mode. Table 44 lists the ECSPI slave mode timing characteristics.

Table 44. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	15 40	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	7 20	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	17	ns

4.7.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 45 shows the interface timing values. The number field in the table refers to timing signals found in Figure 32 and Figure 33.

Table 45. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics[1,2,3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
62	Clock cycle[5]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[6]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[6]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[6]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[6]	— —	— —	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[6]	— —	— —	— —	22.0 12.0	x ck i ck	ns

Table 45. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2,3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [77]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[6]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

1 VCORE_VDD= 1.00 +- 0.10V
Tj = -40C to 125C
CL=50pF

2 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

3 bl = bit length
wl = word length
wr = word length relative

4 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

5 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

6 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

7 Periodically sampled and not 100% tested.

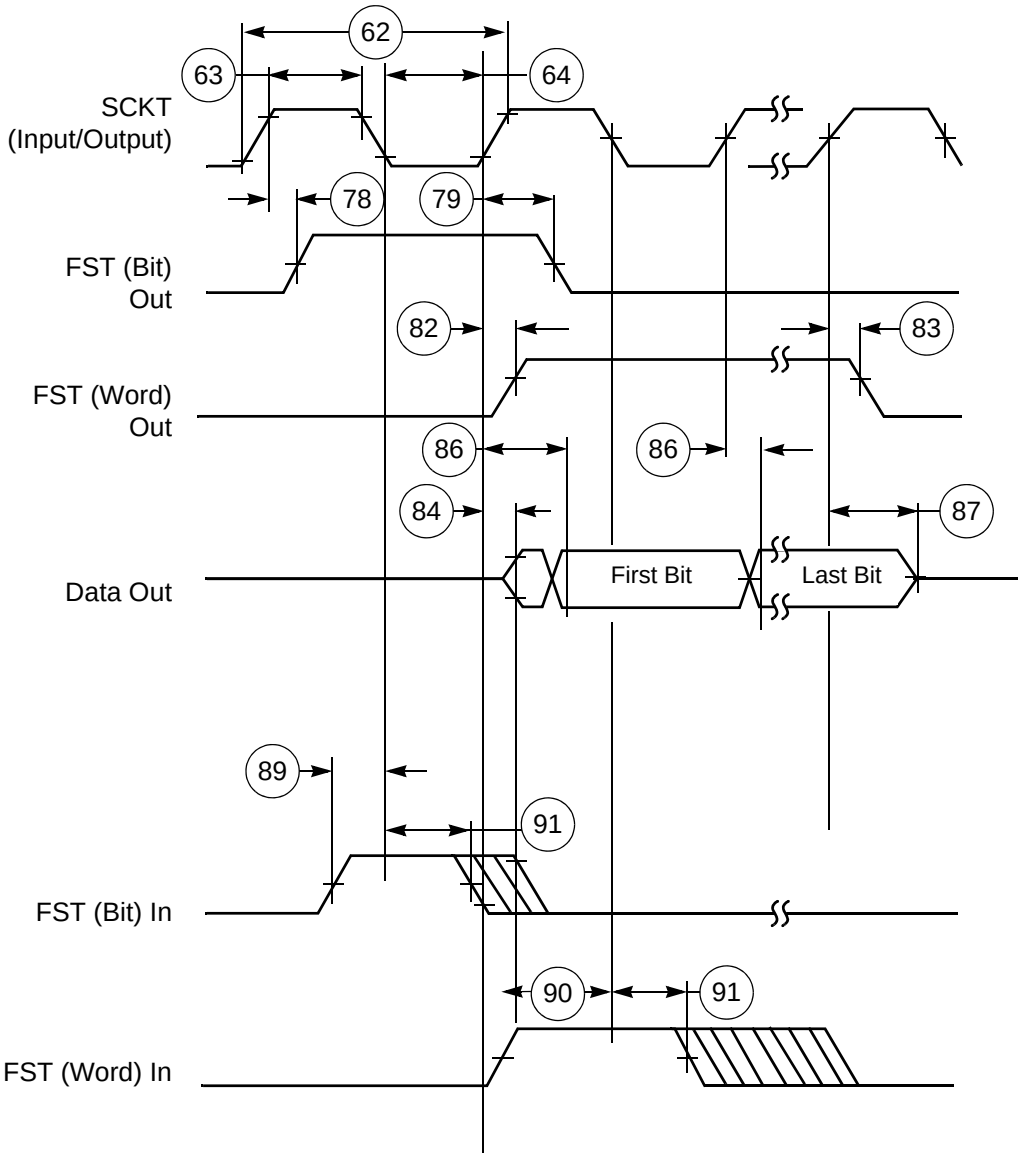


Figure 32. ESAI Transmitter Timing

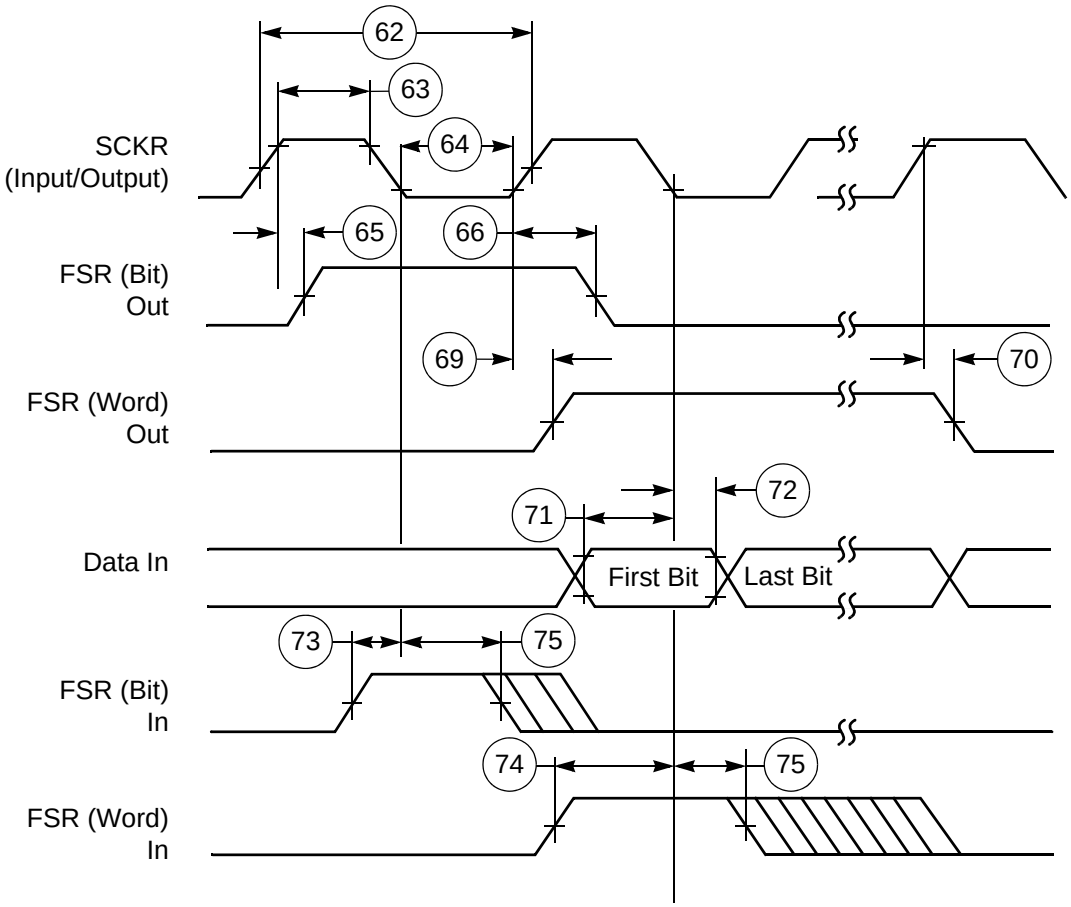


Figure 33. ESAI Receiver Timing

4.7.4 Enhanced Secured Digital Host Controller(eSDHCv2/v3) AC timing

This section describes the electrical information of the eSDHCv2/v3, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.7.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 34 depicts the timing of SD/eMMC4.3, and Table 46 lists the SD/eMMC4.3 timing characteristics.

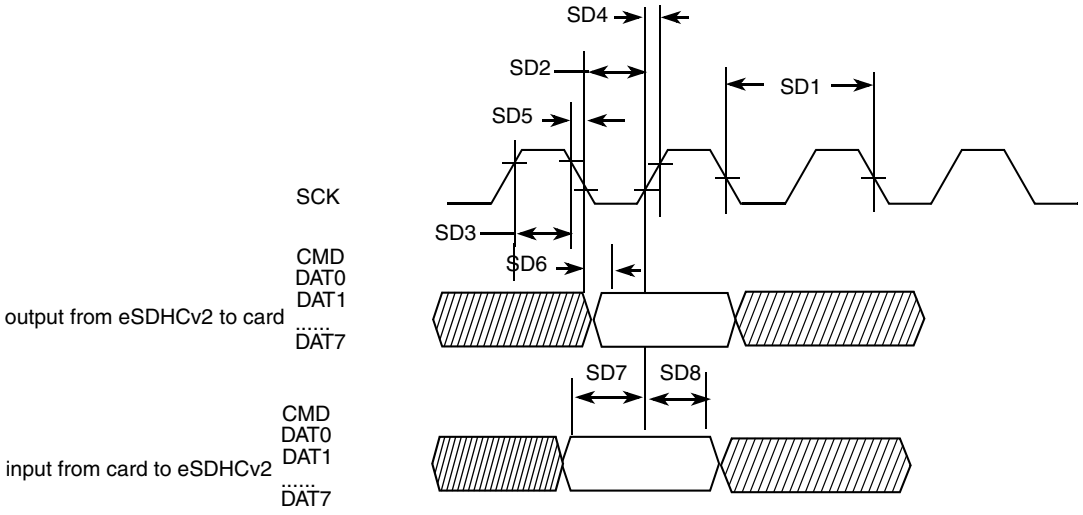


Figure 34. SD/eMMC4.3 Timing

Table 46. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	–5	5	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					

Table 46. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	2.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.7.4.2 eMMC4.4 (Dual Data Rate) eSDHCv3 AC Timing

Figure 35 depicts the timing of eMMC4.4. Table 47 lists the eMMC4.4 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

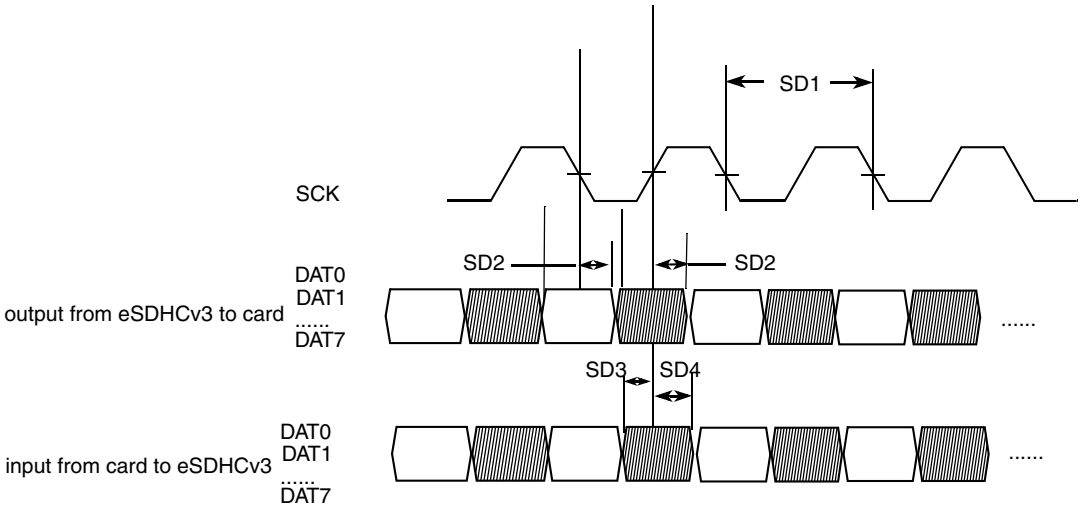


Figure 35. eMMC4.4 Timing

Table 47. eMMC4.4 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}	0	52	MHz
eSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD2	eSDHC Output Delay	t_{OD}	–5	5	ns
eSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					

Table 47. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD3	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD4	eSDHC Input Hold Time	t_{IH}	2.5	—	ns

4.7.5 FEC AC Timing Parameters

This section describes the electrical information of the Fast Ethernet Controller (FEC) module. The FEC is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps MII (18 pins in total) and the 10 Mbps (only 7-wire interface, which uses 7 of the MII pins), for connection to an external Ethernet transceiver. For the pin list of MII and 7-wire, see the i.MX53 Reference Manual.

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.7.5.1 MII Receive Signal Timing

The MII receive signal timing involves the FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK signals. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement but the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 48 lists the MII receive channel signal timing parameters and Figure 36 shows MII receive signal timings.

Table 48. MII Receive Signal Timing

No.	Characteristics[1] [2]	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

1 FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have same timing in 10 Mbps 7-wire interface mode.

2 Test conditions: 25pF on each output signal.

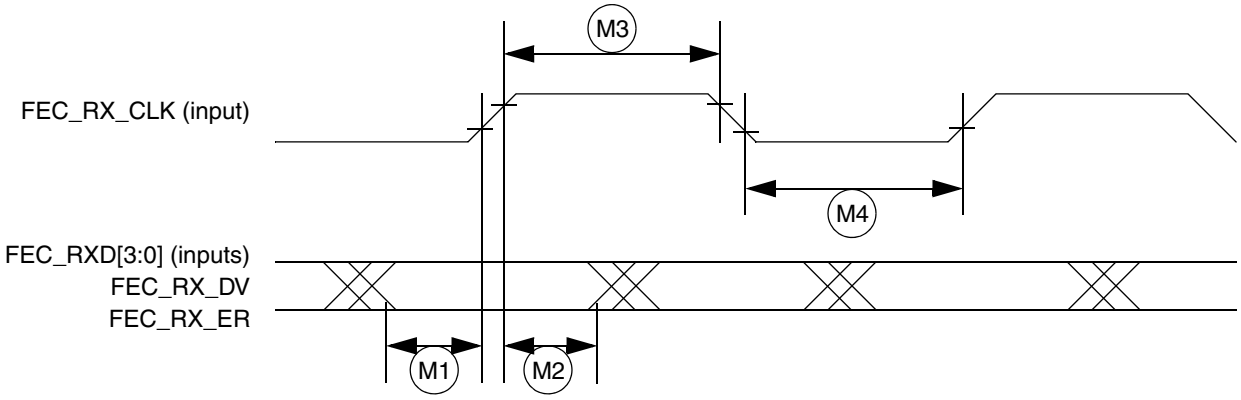


Figure 36. MII Receive Signal Timing Diagram

4.7.5.2 MII Transmit Signal Timing

The MII transmit signal timing affects the FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK signals. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Table 49 lists MII transmit channel timing parameters. Figure 37 shows MII transmit signal timing diagram for the values listed in Table 49.

Table 49. MII Transmit Signal Timing

Num	Characteristic[1] [2]	Min	Max	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

1 FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10 Mbps 7-wire interface mode.

2 Test conditions: 25pF on each output signal.

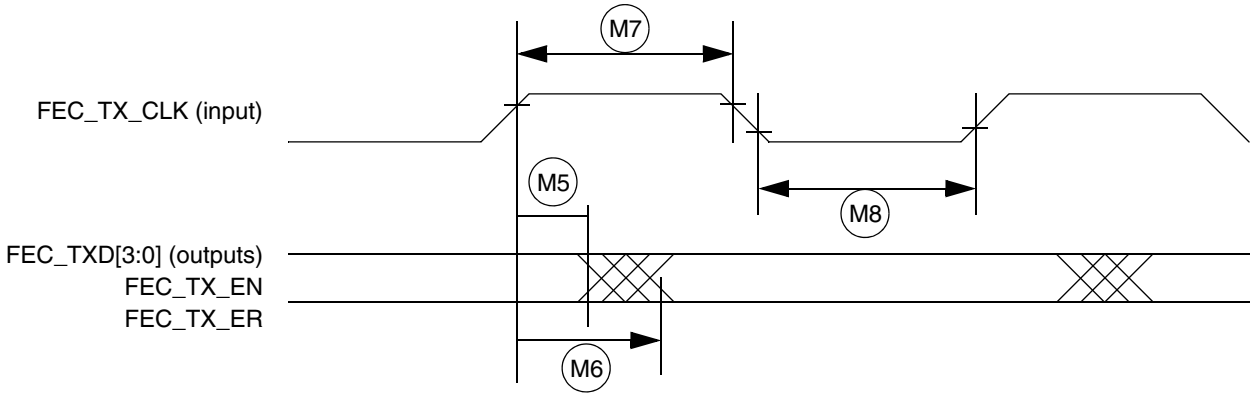


Figure 37. MII Transmit Signal Timing Diagram

4.7.5.3 MII Async Inputs Signal Timing (FEC_CRS and FEC_COL)

Table 50 lists MII asynchronous inputs signal timing information. Figure 38 shows MII asynchronous input timings listed in Table 50.

Table 50. MII Async Inputs Signal Timing

Num	Characteristic [1]	Min	Max	Unit
M9[2]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

1 Test conditions: 25pF on each output signal.

2 FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

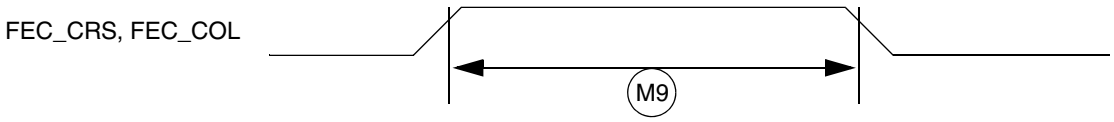


Figure 38. MII Async Inputs Timing Diagram

4.7.5.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 51 lists MII serial management channel timings. Figure 39 shows MII serial management channel timings listed in Table 51. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However, the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 51. MII Transmit Signal Timing

ID	Characteristics[1]	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns

Table 51. MII Transmit Signal Timing (continued)

ID	Characteristics[1]	Min	Max	Unit
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40 %	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40 %	60%	FEC_MDC period

1 Test conditions: 25pF on each output signal.

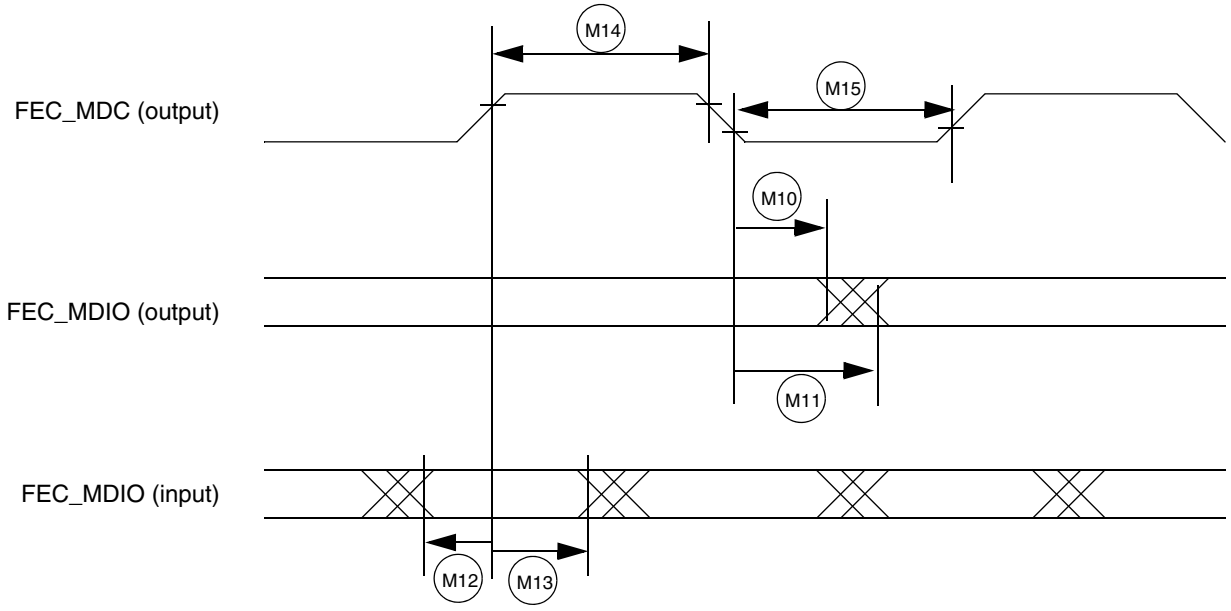


Figure 39. MII Serial Management Channel Timing Diagram

4.7.5.5 RMII Mode Timing

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz ±50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TXD[1:0], FEC_RXD[1:0] and optional FEC_RX_ER.

The RMII mode timings are shown in Table 52 and Figure 40.

Table 52. RMII Signal Timing

No.	Characteristics[1]	Min	Max	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TXD[1:0], FEC_TX_EN invalid	2	—	ns
M19	REF_CLK to FEC_TXD[1:0], FEC_TX_EN valid	—	16	ns

Table 52. RMII Signal Timing (continued)

No.	Characteristics[1]	Min	Max	Unit
M20	FEC_RXD[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	4	—	ns
M21	REF_CLK to FEC_RXD[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

1 Test conditions: 25pF on each output signal.

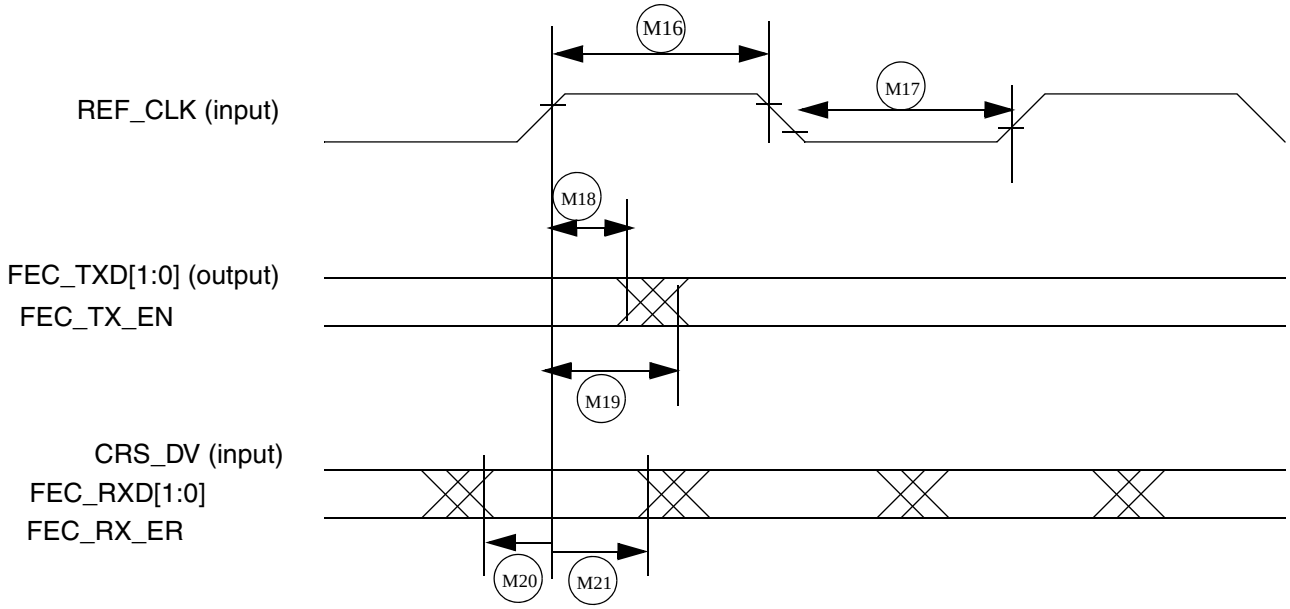


Figure 40. RMII Mode Signal Timing Diagram

4.7.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The electrical characteristics are related to the CAN transceiver external to i.MX53xA such as MC33902 from Freescale.The i.MX53xA has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the i.MX53 reference manual to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

4.7.7 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 41 depicts the timing of I²C module, and Table 53 lists the I²C module timing characteristics.

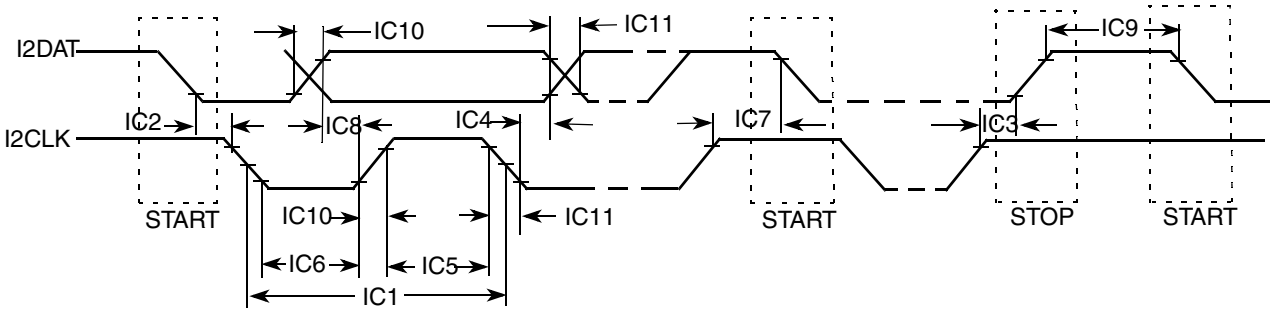


Figure 41. I²C Bus Timing

Table 53. I²C Module Timing Parameters

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.7.8 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.7.8.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 54 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 54. Camera Input Signal Cross Reference, Format and Bits per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr 8 bits 2 cycles	RGB565[4] 16 bits 2 cycles	YCbCr[5] 16 bits 1 cycle	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 20 bits 1 cycle
CSIx_DAT0	—	—	—	—	—	—	—	0	C[0]
CSIx_DAT1	—	—	—	—	—	—	—	0	C[1]
CSIx_DAT2	—	—	—	—	—	—	—	C[0]	C[2]
CSIx_DAT3	—	—	—	—	—	—	—	C[1]	C[3]
CSIx_DAT4	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
CSIx_DAT5	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
CSIx_DAT6	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
CSIx_DAT7	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
CSIx_DAT8	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
CSIx_DAT9	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
CSIx_DAT10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
CSIx_DAT11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
CSIx_DAT12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
CSIx_DAT13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
CSIx_DAT14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
CSIx_DAT15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
CSIx_DAT16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
CSIx_DAT17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
CSIx_DAT18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
CSIx_DAT19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

[1] CSIx stands for CSI1 or CSI2

[2] The MSB bits are duplicated on LSB bits implementing color extension

[3] The two MSB bits are duplicated on LSB bits implementing color extension

[4] RGB 16 bits – supported in two ways: (1) As a “generic data” input – with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.

[5] YCbCr 16 bits - supported as a “generic-data” input – with no on-the-fly processing.

[6] YCbCr 16 bits - supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).

[7] YCbCr, 20 bits, supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.7.8.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.7.8.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.7.8.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 42.

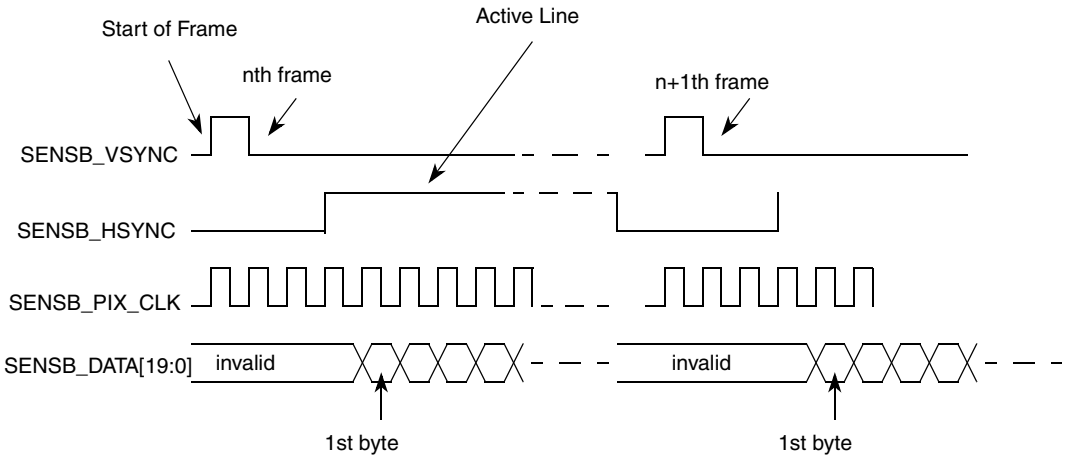


Figure 42. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks.

SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

4.7.8.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.7.8.2.2, "Gated Clock Mode,") except for the SENSB_HSYNC signal, which is not used (see Figure 43). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

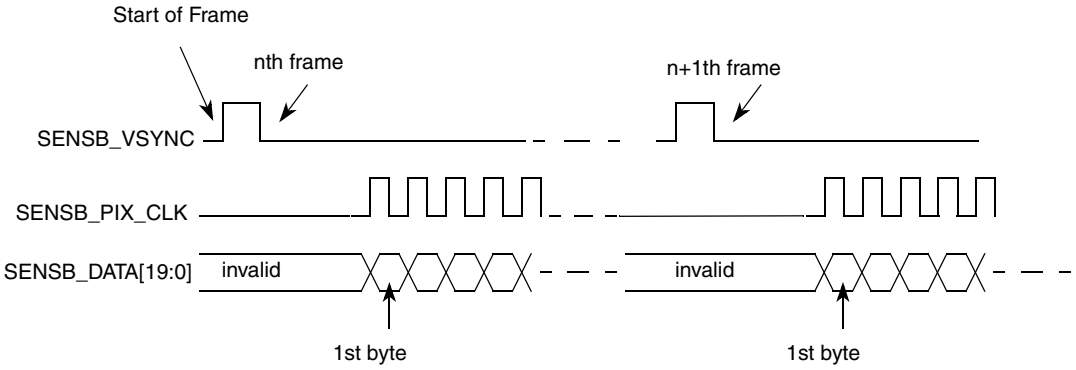


Figure 43. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 43 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.7.8.3 Electrical Characteristics

Figure 44 depicts the sensor interface timing. SENSB_MCLK signal described here is not generated by the IPU. Table 55 lists the sensor interface timing characteristics.

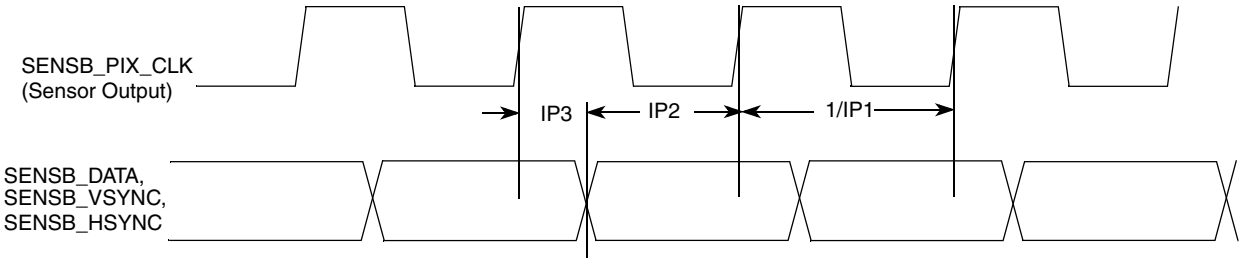


Figure 44. Sensor Interface Timing Diagram

Table 55. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.7.8.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 56 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 56. Video Signal Cross-Reference

i.MX53xA	LCD							Comment[1]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	DAT[0]	The restrictions are as follows: a) There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. b) The bit order is expressed in each of the bit groups, for example B[0] = least significant blue pixel bit
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	DAT[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	DAT[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	DAT[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	DAT[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	DAT[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	DAT[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	DAT[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	DAT[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	DAT[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	DAT[10]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	DAT[11]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	DAT[12]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	DAT[13]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	DAT[14]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	DAT[15]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—	

Table 56. Video Signal Cross-Reference (continued)

i.MX53xA	LCD								Comment[1]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart	
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name	
DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—	—
DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—	—
DIx_DISP_CLK	PixCLK							—	—
DIx_PIN1	—							VSYNC_IN	May be required for anti-tearing
DIx_PIN2	HSYNC							—	—
DIx_PIN3	VSYNC							—	VSYNC out
DIx_PIN4	—							—	Additional frame/row synchronous signals with programmable timing
DIx_PIN5	—							—	
DIx_PIN6	—							—	
DIx_PIN7	—							—	
DIx_PIN8	—							—	
DIx_D0_CS	—							CS0	—
DIx_D1_CS	—							CS1	Alternate mode of PWM output for contrast or brightness control
DIx_PIN11	—							WR	—
DIx_PIN12	—							RD	—
DIx_PIN13	—							RS1	Register select signal
DIx_PIN14	—							RS2	Optional RS2
DIx_PIN15	DRDY/DV							DRDY	Data validation/blank, data enable
DIx_PIN16	—							—	Additional data synchronous signals with programmable features/timing
DIx_PIN17	Q							—	

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 56 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.7.8.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.7.8.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as HSYNC/VSYCN and so on) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the i.MX53 Reference Manual.

4.7.8.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.7.8.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.7.8.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point.

4.7.8.6.2 LCD Interface Functional Description

Figure 45 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock, used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

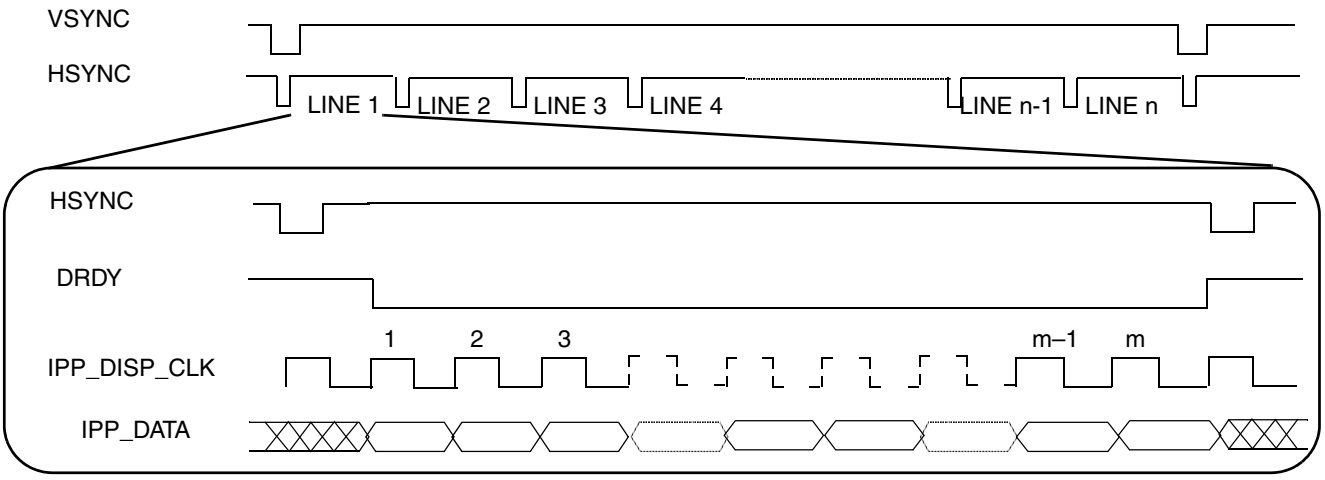


Figure 45. Interface Timing Diagram for TFT (Active Matrix) Panels

4.7.8.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 46 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

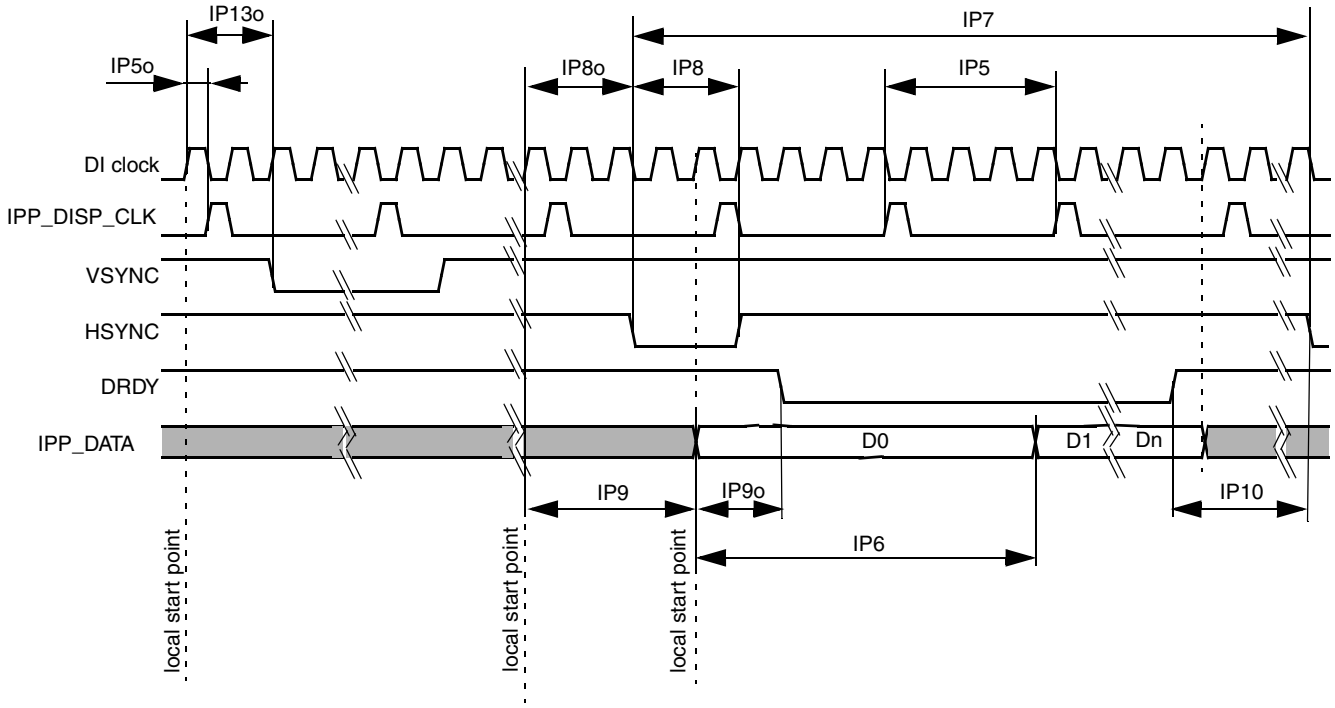


Figure 46. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 47 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

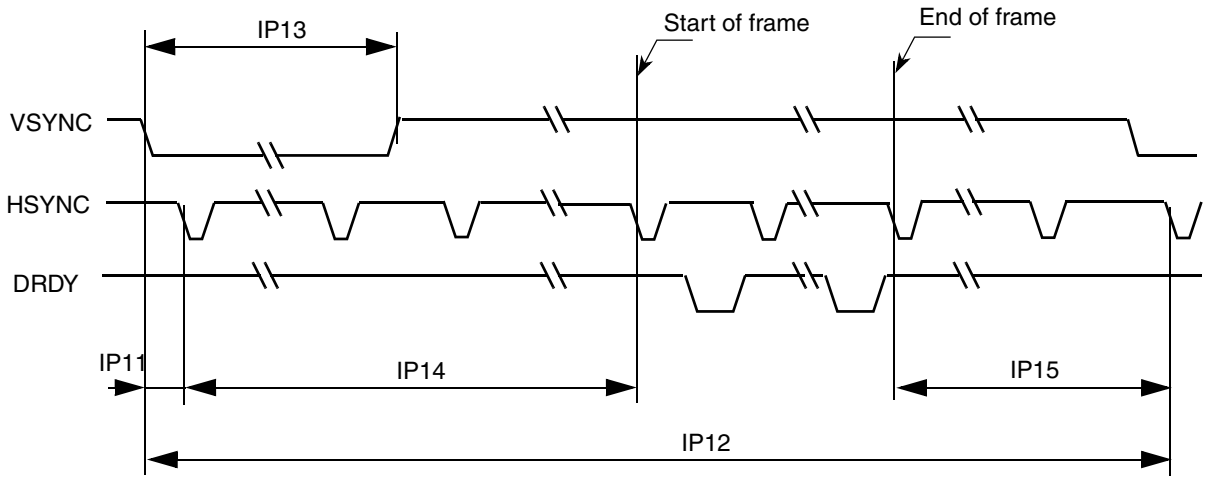


Figure 47. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 57 shows timing characteristics of signals presented in Figure 46 and Figure 47.

Table 57. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line.The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) × Tsw	Width of second Vertical blanking interval in line.The FH should be built by suitable DI's counter.	ns

Table 57. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution) Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution) The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \dfrac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}, & \text{for integer } \dfrac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \\ T_{diclk}\left(floor\left[\dfrac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \dfrac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}dicp = T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

The maximal accuracy of UP/DOWN edge of IPP_DATA is:

$$\text{Accuracy} = T_{diclk} \pm 0.62\text{ns}$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed through the registers.

Figure 48 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set through the Register. Table 58 lists the synchronous display interface timing characteristics.

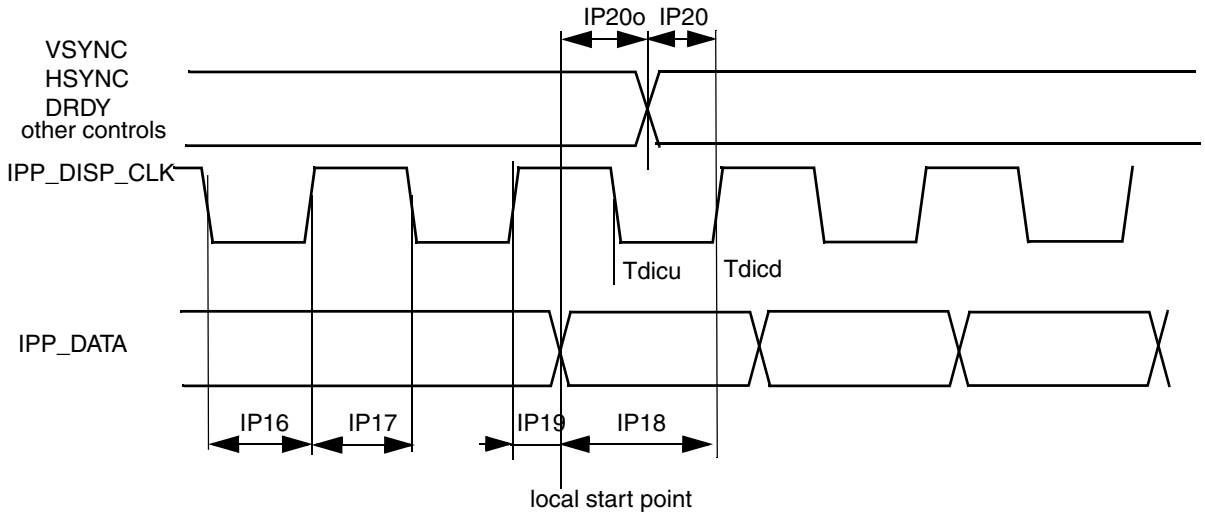


Figure 48. Synchronous Display Interface Timing Diagram—Access Level

Table 58. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu–1.24	Tdicd[2]–Tdicu[3]	Tdicd–Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.24	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd–1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–1.24	Tdicp–Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu–1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd–1.24–Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$Tdicd = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP_CLK_DOWN}{DI_CLK_PERIOD}\right]\right)$$

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$Tdicu = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP_CLK_UP}{DI_CLK_PERIOD}\right]\right)$$

4.7.8.7 Interface to a TV Encoder (TVDAC)

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The timing of the interface is described in Figure 49.

NOTE

- The frequency of the clock DISP_CLK is 27 MHz (within 10%)
- The HSYNC, VSYNC signals are active low.
- The DRDY signal is shown as active high.
- The transition to the next row is marked by the negative edge of the HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the VSYNC signal. It remains low for at least one clock cycles.

  — At a transition to an odd field (of the next frame), the negative edges of VSYNC and HSYNC coincide.

  — At a transition is to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the HSYNC signal being high.

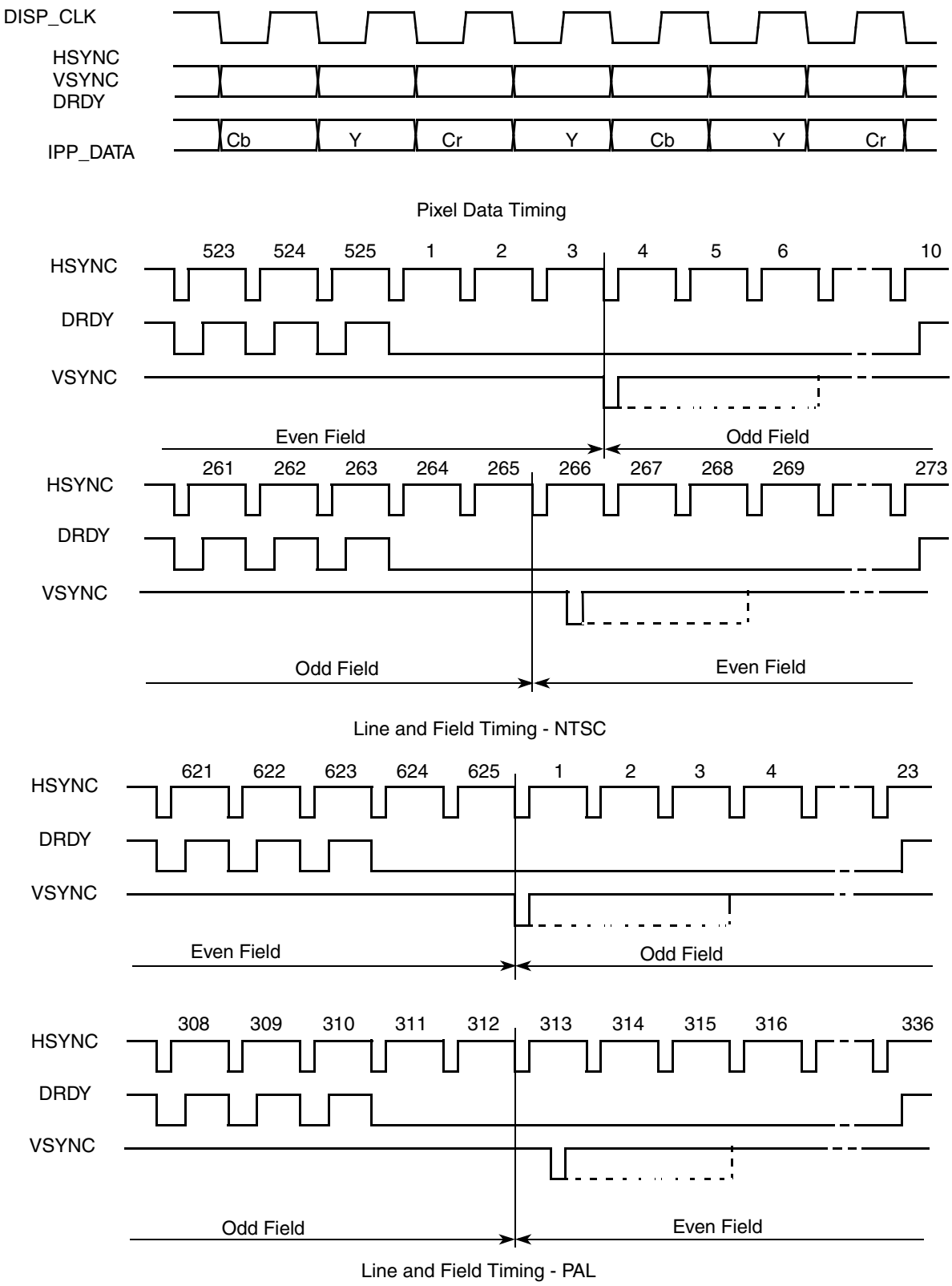


Figure 49. TV Encoder Interface Timing Diagram

4.7.8.7.1 TVEv2 TV Encoder Performance Specifications

The TV encoder output specifications are shown in Table 59. All the parameters in the table are defined under the following conditions:

- R_{set} = 1.05 kΩ ±1%, resistor on TVDAC_VREF pin to GND
- R_{load} = 37.5 Ω ±1%, output load to the GND

Table 59. TV Encoder Video Performance Specifications

Parameter	Conditions	Min	Typ	Max	Unit
DAC STATIC PERFORMANCE					
Resolution[1]	—	—	10	—	Bits
Integral Nonlinearity (INL)[2]	—	—	1	2	LSBs
Differential Nonlinearity (DNL) [2]	—	—	0.6	1	LSBs
Channel-to-channel gain matching[2]	—	—	2	—	%
Full scale output voltage[2]	R_{set} = 1.05 kΩ ±1% R_{load} = 37.5 Ω ±1%	1.24	1.306	1.37	V
DAC DYNAMIC PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	F_{out} = 3.38 MHz F_{samp} = 216 MHz	—	59	—	dBc
Spurious Free Dynamic Range (SFDR)	F_{out} = 9.28 MHz F_{samp} = 297 MHz	—	54	—	dBc
VIDEO PERFORMANCE IN SD MODE[2]					
Short Term Jitter (Line to Line)	—	—	2.5	—	±ns
Long Term Jitter (Field to Field)	—	—	3.5	—	±ns
Frequency Response	0-4.0 MHz	–0.1	—	0.1	dB
	5.75 MHz	–0.7	—	0	dB
Luminance Nonlinearity	—	—	0.5	—	±%
Differential Gain	—	—	0.35	—	%
Differential Phase	—	—	0.6	—	Degrees
Signal-to-Noise Ratio (SNR)	Flat field full bandwidth	—	75	—	dB
Hue Accuracy	—	—	0.8	—	±Degrees
Color Saturation Accuracy	—	—	1.5	—	±%
Chroma AM Noise	—	—	–70	—	dB
Chroma PM Noise	—	—	–47	—	dB
Chroma Nonlinear Phase	—	—	0.5	—	±Degrees
Chroma Nonlinear Gain	—	—	2.5	—	±%
Chroma/Luma Intermodulation	—	—	0.1	—	±%
Chroma/Luma Gain Inequality	—	—	1.0	—	±%

Table 59. TV Encoder Video Performance Specifications (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Chroma/Luma Delay Inequality	—	—	1.0	—	±ns
VIDEO PERFORMANCE IN HD MODE[2]					
Luma Frequency Response	0-30 MHz	–0.2	—	0.2	dB
Chroma Frequency Response	0-15 MHz, YCbCr 422 mode	–0.2	—	0.2	dB
Luma Nonlinearity	—	—	3.2	—	%
Chroma Nonlinearity	—	—	3.4	—	%
Luma Signal-to-Noise Ratio	0-30 MHz	—	62	—	dB
Chroma Signal-to-Noise Ratio	0-15 MHz	—	72	—	dB

1 Guaranteed by design.

2 Guaranteed by characterization.

4.7.8.8 Asynchronous Interfaces

The following sections describes the types of asynchronous interfaces.

4.7.8.8.1 Standard Parallel Interfaces

The IPU has four signal generator machines for asynchronous signal. Each machine generates IPU's internal control levels (0 or 1) by UP and DOWN that are defined in registers. Each asynchronous pin has a dynamic connection with one of the signal generators. This connection is redefined again with a new display access (pixel/component). The IPU can generate control signals according to system 80/68 requirements. The burst length is received as a result from predefined behavior of the internal signal generator machines.

The access to a display is realized by the following:

- CS (IPP_CS) chip select
- WR (IPP_PIN_11) write strobe
- RD (IPP_PIN_12) read strobe
- RS (IPP_PIN_13) Register select (A0)

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 50, Figure 51, Figure 52, and Figure 53. The timing images correspond to active-low IPP_CS, WR and RD signals.

Each asynchronous access is defined by an access size parameter. This parameter can be different between different kinds of accesses. This parameter defines a length of windows, when suitable controls of the current access are valid. A pause between two different display accesses can be guaranteed by programing suitable access sizes. There are no minimal/maximal hold/setup times hard defined by DI. Each control signal can be switched at any time during access size.

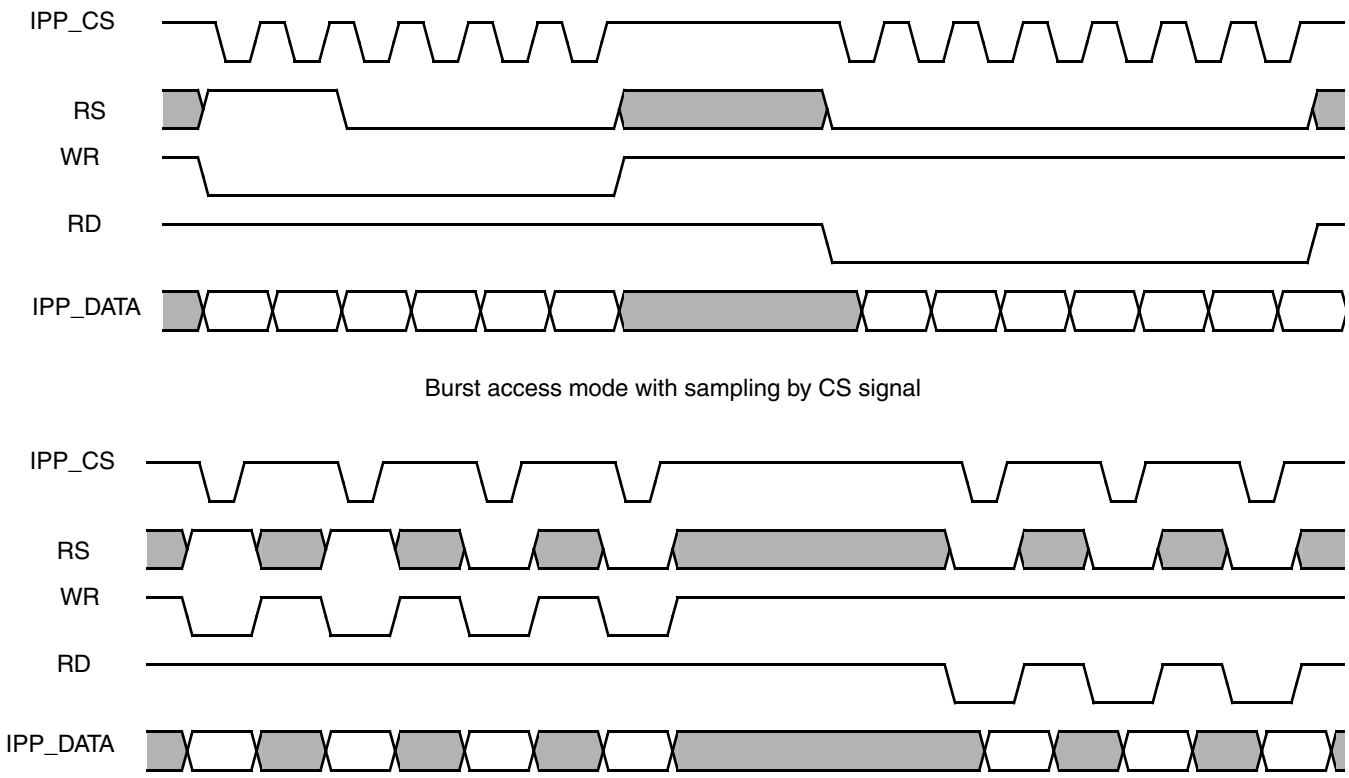


Figure 50. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

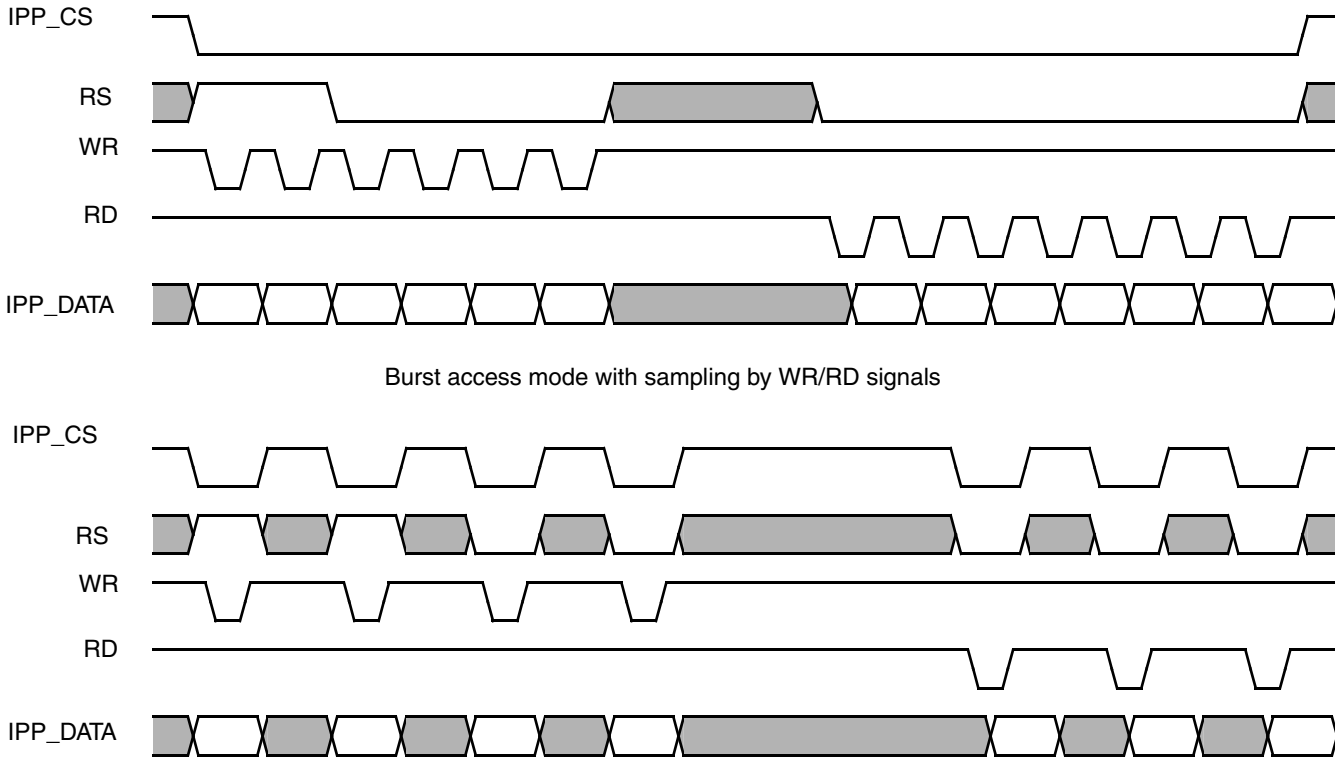


Figure 51. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

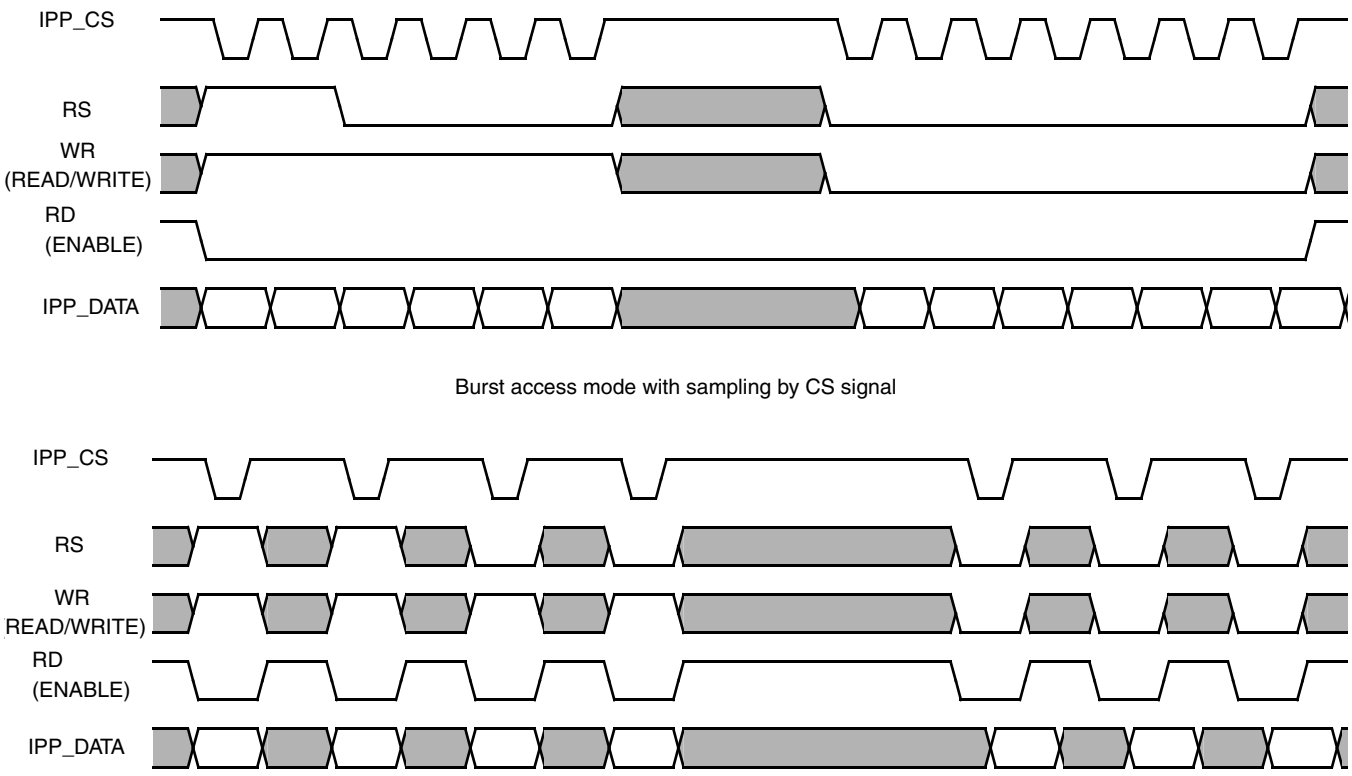


Figure 52. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

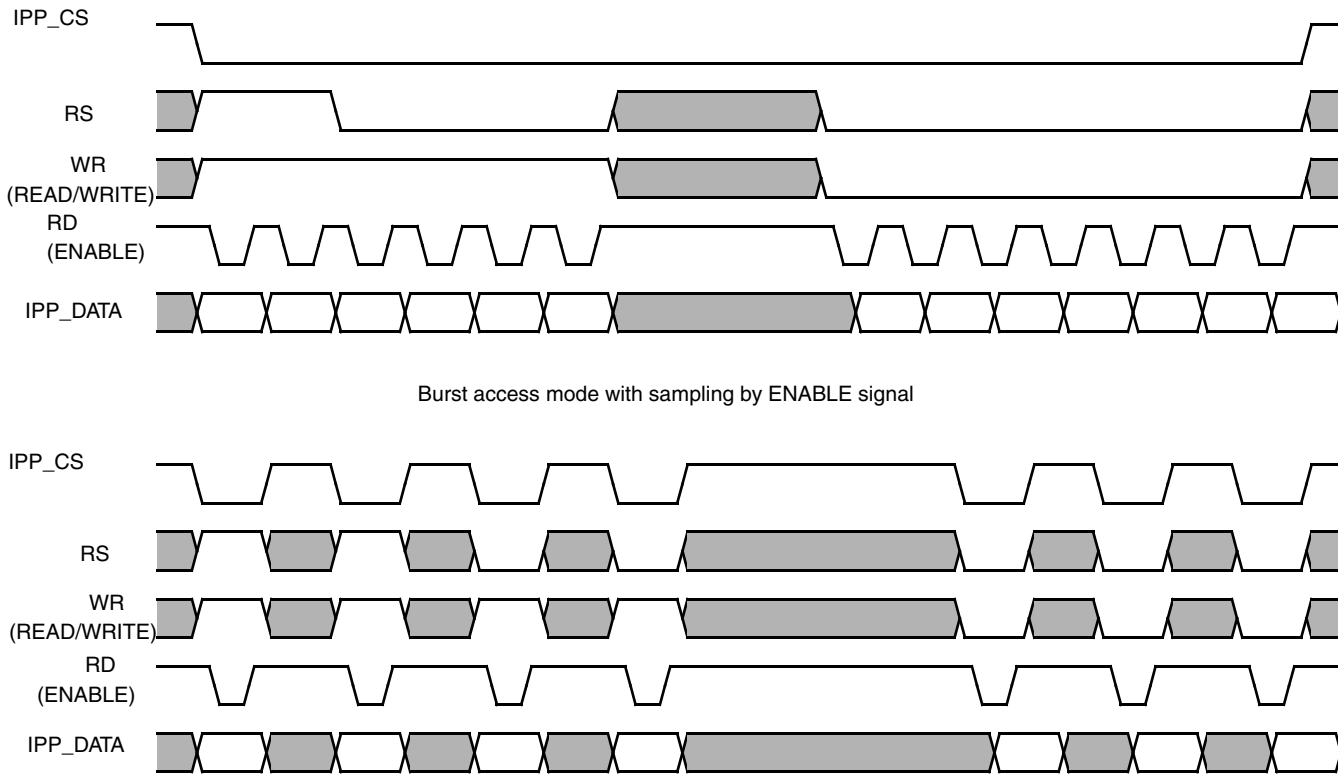


Figure 53. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Display operation can be performed with IPP_WAIT signal. The DI reacts to the incoming IPP_WAIT signal with 2 DI_CLK delay. The DI finishes a current access and a next access is postponed until IPP_WAIT release. Figure 54 shows timing of the parallel interface with IPP_WAIT control.

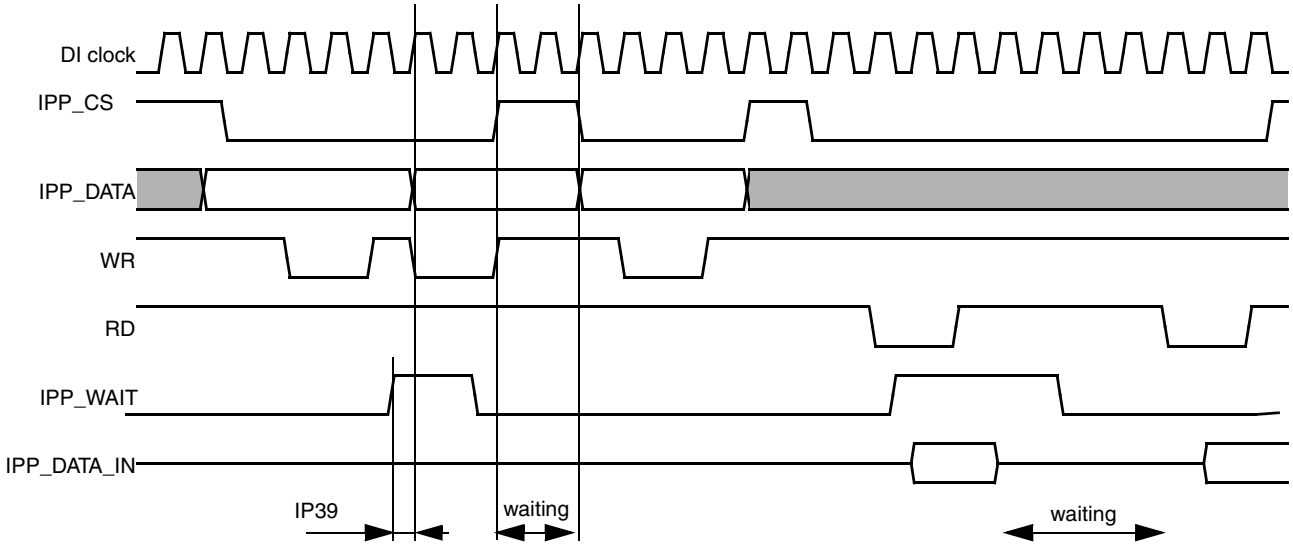


Figure 54. Parallel Interface Timing Diagram—Read Wait States

4.7.8.8.2 Asynchronous Parallel Interface Timing Parameters

Figure 55 depicts timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 61 shows timing characteristics at display access level. All timing diagrams are based on active low control signals (signals polarity is controlled through the DI_DISP_SIG_POL register).

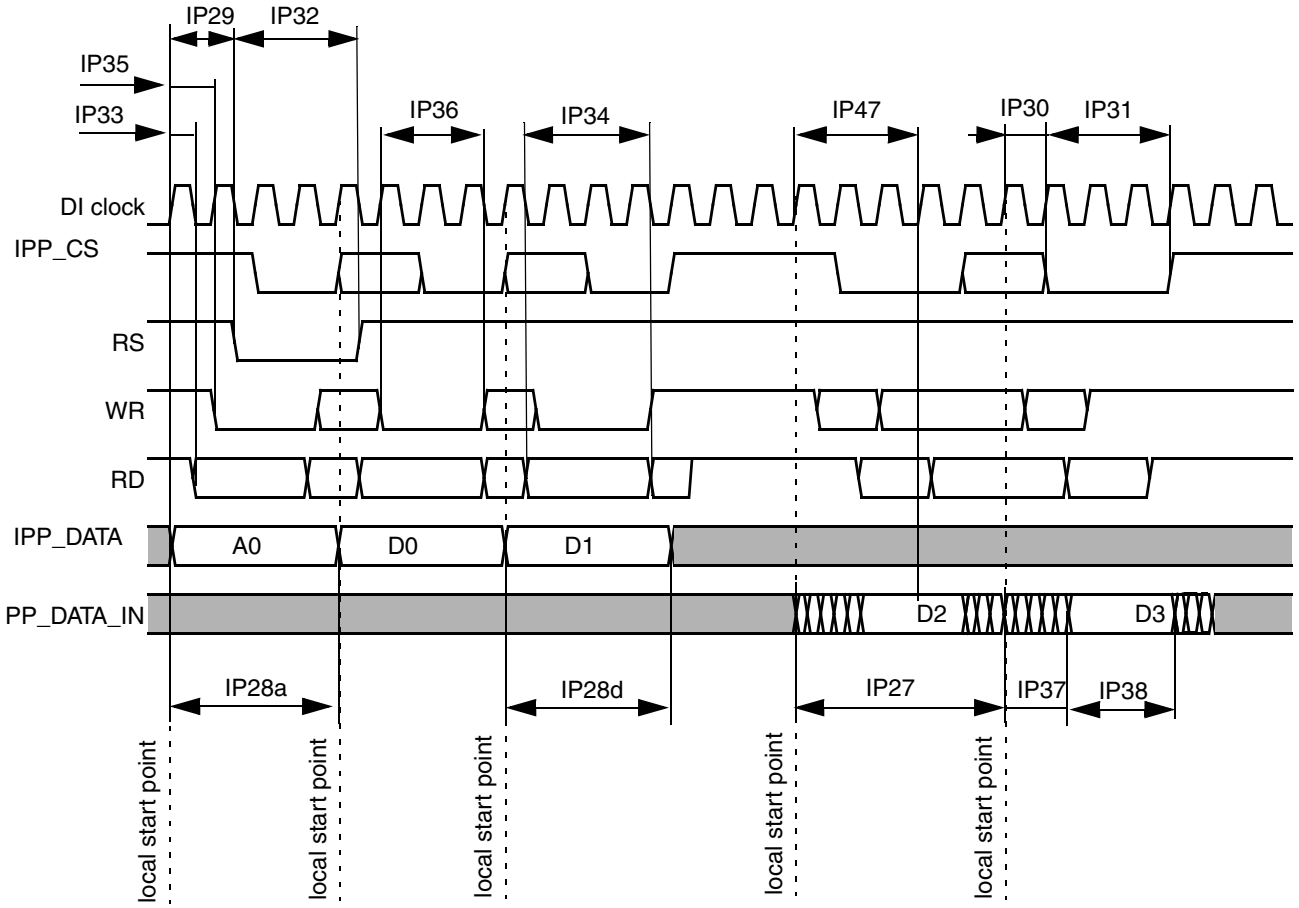


Figure 55. Asynchronous Parallel Interface Timing Diagram

Table 60. Asynchronous Display Interface Timing Parameters (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP27	Read system cycle time	Tcycr	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28a	Address Write system cycle time	Tcycwa	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28d	Data Write system cycle time	Tcycwd	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP29	RS start	Tdcsrr	UP#	RS strobe switch, predefined value in DI REGISTER	ns
IP30	CS start	Tdcsc	UP#	CS strobe switch, predefined value in DI REGISTER	ns
IP31	CS hold	Tdchc	DOWN#	CS strobe release, predefined value in DI REGISTER	—
IP32	RS hold	Tdchrr	DOWN#	RS strobe release, predefined value in DI REGISTER	—
IP33	Read start	Tdcsr	UP#	read strobe switch, predefined value in DI REGISTER	ns

Table 60. Asynchronous Display Interface Timing Parameters (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP34	Read hold	Tdchr	DOWN#	read strobe release signal, predefined value in DI REGISTER	ns
IP35	Write start	Tdcsw	UP#	write strobe switch, predefined value in DI REGISTER	ns
IP36	Controls hold time for write	Tdchw	DOWN#	write strobe release, predefined value in DI REGISTER	ns
IP37	Slave device data delay[1]	Tracc	Delay of incoming data	Physical delay of display's data, defined from Read access local start point	ns
IP38	Slave device data hold time	Troh	Hold time of data on the buss	Time that display read data is valid in input bus	ns
IP47	Read time point	Tdrp	Data sampling point	Point of input data sampling by DI, predefined in DC Microcode	—

[1]This parameter is a requirement to the display connected to the IPU.

Table 61. Asynchronous Parallel Interface Timing Parameters (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP27	Read system cycle time	Tcycr	Tdicpr – 1.24	Tdicpr[2]	Tdicpr+1.24	ns
IP28	Write system cycle time	Tcycw	Tdicpw – 1.24	Tdicpw[3]	Tdicpw+1.24	ns
IP29	RS start	Tdcsrr	Tdicurs – 1.24	Tdicurs	Tdicurs+1.24	ns
IP30	CS start	Tdcsc	Tdicucs – 1.24	Tdicur	Tdicucs+1.24	ns
IP31	CS hold	Tdchc	Tdicdcs – Tdicucs – 1.24	Tdicdcs[4]–Tdicucs[5]	Tdicdcs – Tdicucs+1.24	ns
IP32	RS hold	Tdchrr	Tdicdrs – Tdicurs – 1.24	Tdicdrs[6]–Tdicurs[7]	Tdicdrs – Tdicurs+1.24	ns
IP33	Controls setup time for read	Tdcsr	Tdicur – 1.24	Tdicur	Tdicur+1.24	ns
IP34	Controls hold time for read	Tdchr	Tdicdr – Tdicur – 1.24	Tdicdr[8]–Tdicur[9]	Tdicdr – Tdicur+1.24	ns
IP35	Controls setup time for write	Tdcsw	Tdicuw – 1.24	Tdicuw	Tdicuw+1.24	ns
IP36	Controls hold time for write	Tdchw	Tdicdw – Tdicuw – 1.24	Tdicpw[10]–Tdicuw[11]	Tdicdw–Tdicuw+1.24	ns
IP37	Slave device data delay[12]	Tracc	0	—	Tdrp[13] – Tlbd[14] –Tdicur–1.24	ns
IP38	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr+1.24	—	Tdicpr – Tdicdr – 1.24	ns

Table 61. Asynchronous Parallel Interface Timing Parameters (Access Level) (continued)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP39	Setup time for wait signal	Tswait	—	—	—	—
IP47	Read time point	Tdrp	Tdrp – 1.24	Tdrp	Tdrp+1.24	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2]Display period value for read

$$Tdicpr = T_{DI_CLK} \times ceil\left[\frac{DI_ACCESS_SIZE_\#}{DI_CLK_PERIOD}\right]$$

ACCESS_SIZE is predefined in REGISTER.

[3]Display period value for write

$$Tdicpw = T_{DI_CLK} \times ceil\left[\frac{DI_ACCESS_SIZE_\#}{DI_CLK_PERIOD}\right]$$

ACCESS_SIZE is predefined in REGISTER.

[4]Display control down for CS

$$Tdicdcs = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER.

[5]Display control up for CS

$$Tdicucs = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER.

[6]Display control down for RS

$$Tdicdrs = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER.

[7]Display control up for RS

$$Tdicurs = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER.

[8]Display control down for read

$$Tdicdr = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER.

[9]Display control up for read

$$Tdicur = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER.

[10]Display control down for read

$$Tdicdrw = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER.

[11]Display control up for write

$$Tdicuw = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER.

[12]This parameter is a requirement to the display connected to the IPU.

[13]Data read point

$$Tdrp = T_{DI_CLK} \times ceil\left[\frac{DISP\#_READ_EN}{DI_CLK_PERIOD}\right]$$

Note: DISP#_READ_EN—operand of DC's MICROCDE READ command to sample incoming data.

[14]Loop back delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a chip-level output delay, board delays, a chip-level input delay, an IPU input delay. This value is chip specific.

4.7.8.9 Standard Serial Interfaces

The IPU supports the following types of asynchronous serial interfaces:

1. 3-wire (with bidirectional data line).
2. 4-wire (with separate data input and output lines).
3. 5-wire type 1 (with sampling RS by the serial clock).
4. 5-wire type 2 (with sampling RS by the chip select signal).

The IPU has four independent outputs and one input. The port can be configured to provide 3, 4, or 5-wire interfaces.

Figure 56 depicts the timing diagram of the 3-wire serial interface. The timing diagrams correspond to active-low IPP#_CS signal and the straight polarity of the IPP_CLK signal.

For this interface, a bidirectional data line is used outside the chip. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux should provide joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

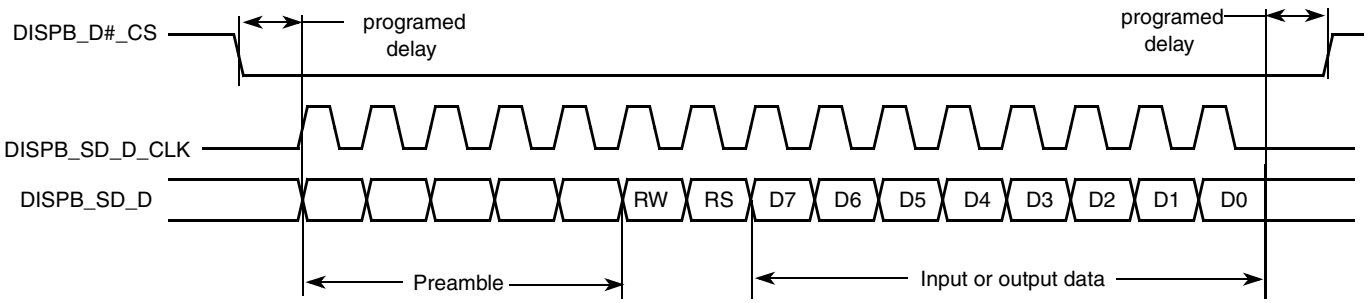


Figure 56. 3-Wire Serial Interface Timing Diagram

Figure 57 depicts timing diagram of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the chip.

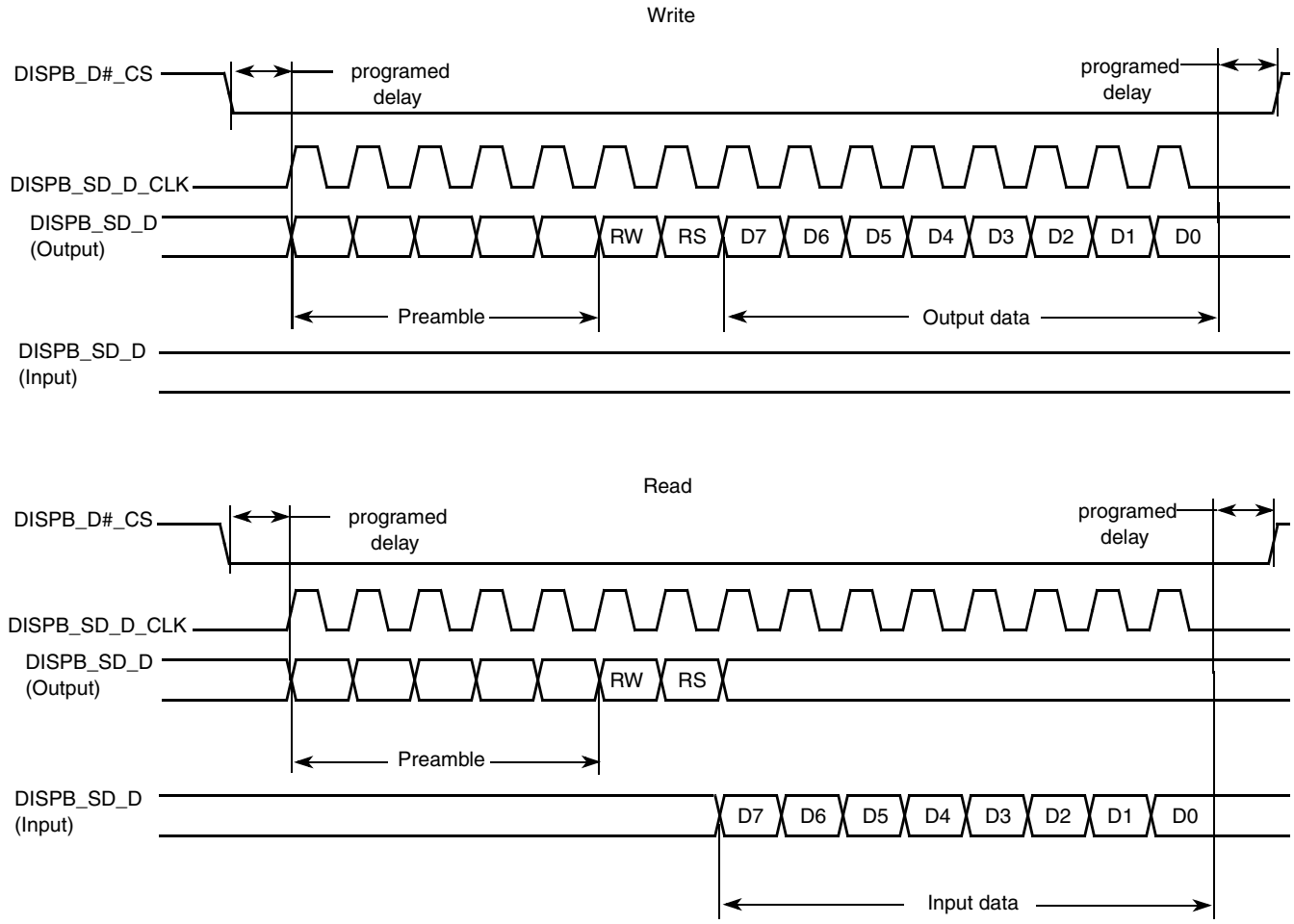


Figure 57. 4-Wire Serial Interface Timing Diagram

Figure 58 depicts timing of the 5-wire serial interface. For this interface, a separate RS line is added.

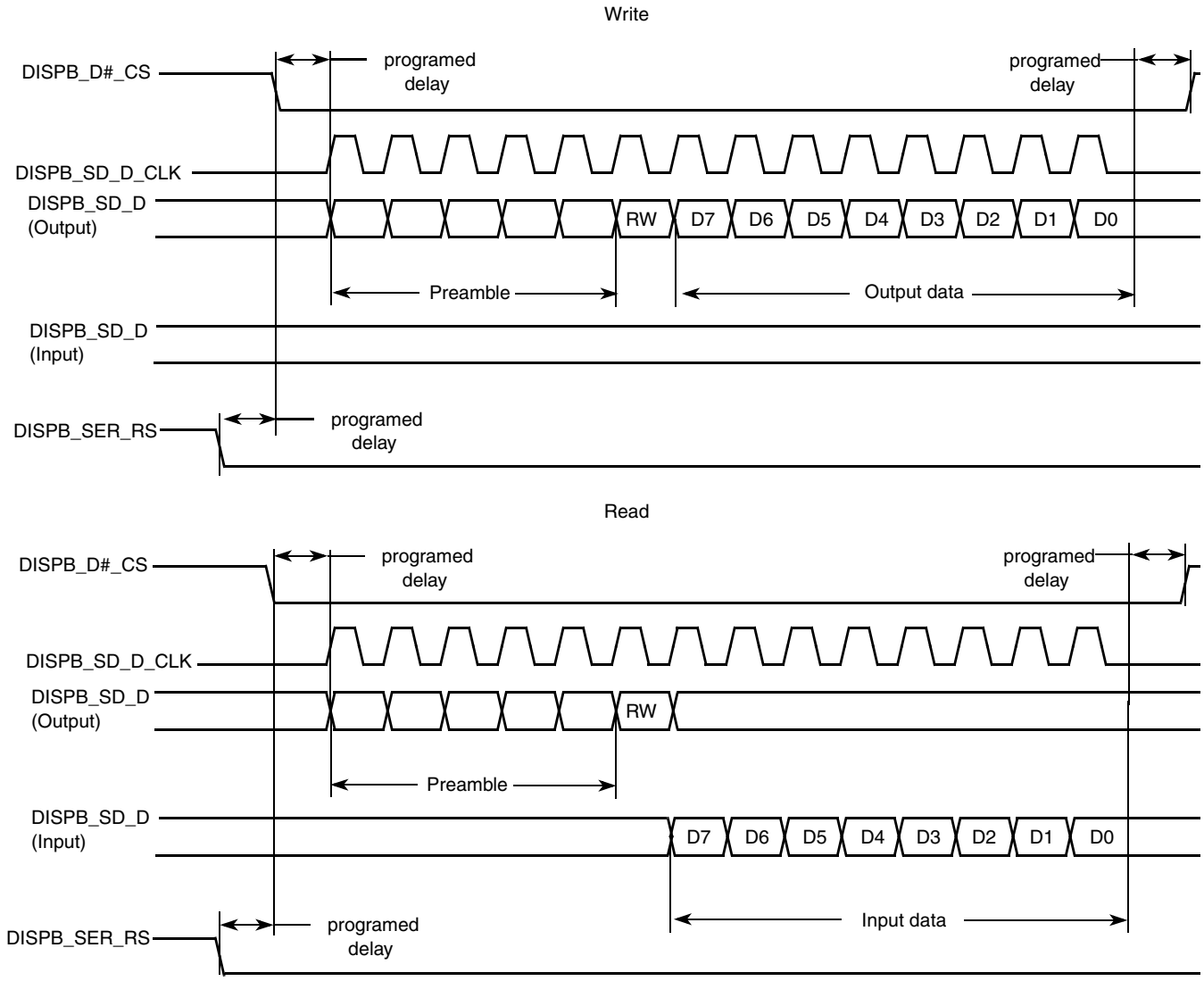


Figure 58. 5-Wire Serial Interface Timing Diagram

4.7.8.9.1 Asynchronous Serial Interface Timing Parameters

Figure 59 depicts timing of the serial interface. Table 62 shows timing characteristics at display access level.

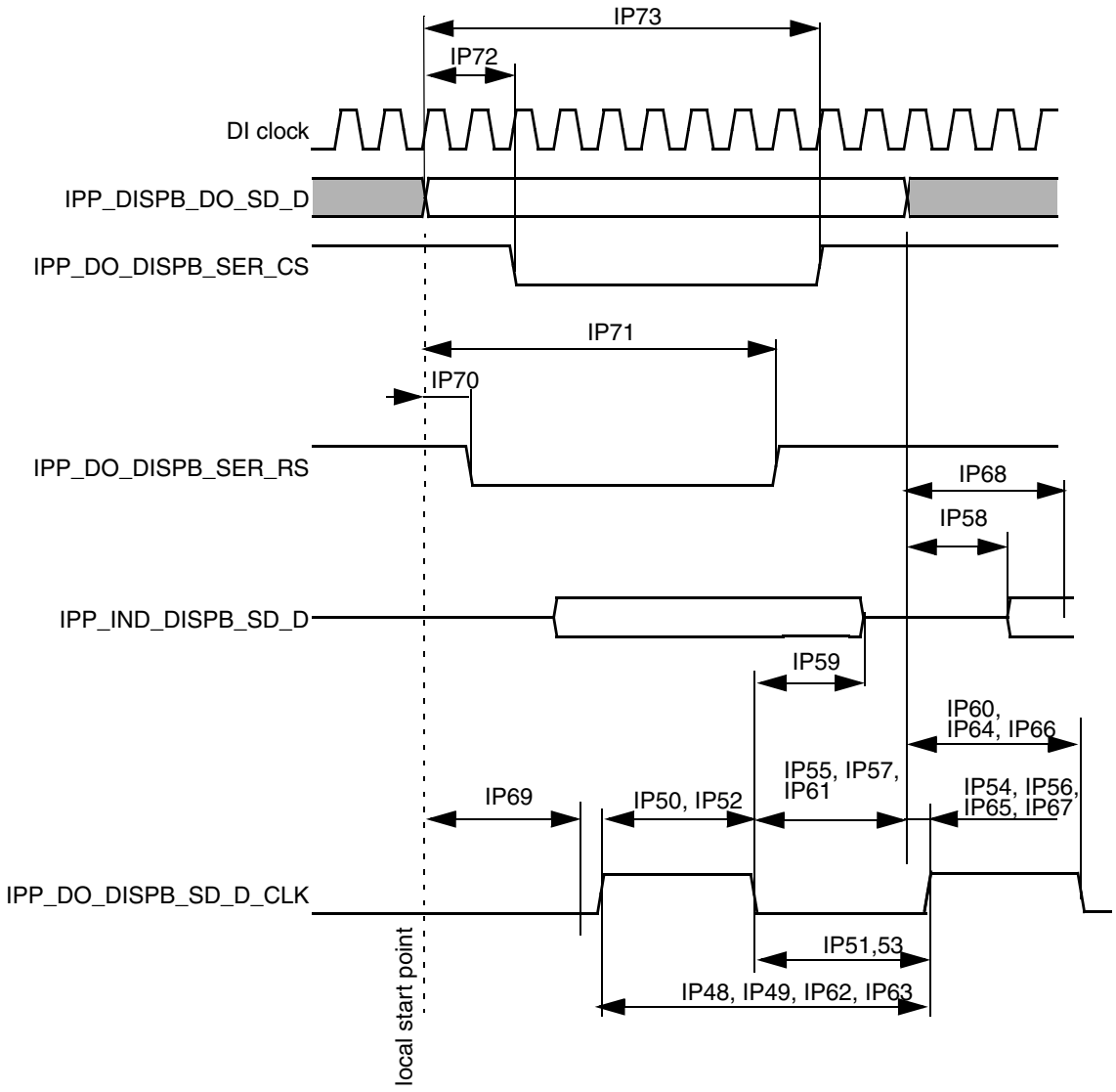


Figure 59. Asynchronous Serial Interface Timing Diagram

Table 62. Asynchronous Serial Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP48	Read system cycle time	Tcycr	Tdicpr–1.24	Tdicpr[2]	Tdicpr+1.24	ns
IP49	Write system cycle time	Tcycw	Tdicpw–1.24	Tdicpw[3]	Tdicpw+1.24	ns
IP50	Read clock low pulse width	Trl	Tdicdr–Tdicur–1.24	Tdicdr[4]–Tdicur[5]	Tdicdr–Tdicur+1.24	ns
IP51	Read clock high pulse width	Trh	Tdicpr–Tdicdr+Tdicur–1.24	Tdicpr–Tdicdr+Tdicur	Tdicpr–Tdicdr+Tdicur+1.24	ns

Table 62. Asynchronous Serial Interface Timing Characteristics (Access Level) (continued)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP52	Write clock low pulse width	Twl	Tdicdw – Tdicuw – 1.24	Tdicdw[6] –Tdicuw[7]	Tdicdw – Tdicuw+1.24	ns
IP53	Write clock high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.24	Tdicpw–Tdicdw+ Tdicuw	Tdicpw – Tdicdw+ Tdicuw+1.24	ns
IP54	Controls setup time for read	Tdcsr	Tdicur–1.24	Tdicur	—	ns
IP55	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.24	Tdicpr – Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw – 1.24	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.24	Tdicpw–Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.24	ns
IP59	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr+1.24	—	Tdicpr – Tdicdr – 1.24	ns
IP60	Write data setup time	Tds	Tdicdw – 1.24	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.24	Tdicpw – Tdicdw	—	ns
IP62	Read period	Tdicpr	Tdicpr – 1.24	Tdicpr	Tdicpr+1.24	ns
IP63	Write period	Tdicpw	Tdicpw – 1.24	Tdicpw	Tdicpw+1.24	ns
IP64	Read down time	Tdicdr	Tdicdr – 1.24	Tdicdr	Tdicdr+1.24	ns
IP65	Read up time	Tdicur	Tdicur – 1.24	Tdicur	Tdicur+1.24	ns
IP66	Write down time	Tdicdw	Tdicdw – 1.24	Tdicdw	Tdicdw+1.24	ns
IP67	Write up time	Tdicuw	Tdicuw – 1.24	Tdicuw	Tdicuw+1.24	ns
IP68	Read time point	Tdrp	Tdrp – 1.24	Tdrp	Tdrp+1.24	ns
IP69	Clock offset[11]	Toclk	Toclk – 1.24	Toclk	Toclk+1.24	ns
IP70	RS up time[12]	Tdicurs	Tdicurs– 1.24	Tdicurs	Tdicurs+1.24	ns
IP71	RS down time[13]	Tdicdrs	Tdicdrs – 1.24	Tdicdrs	Tdicdrs+1.24	ns
IP72	CS up time[14]	Tdicucs	Tdicucs – 1.24	Tdicucs	Tdicucs+1.24	ns
IP73	CS down time[15]	Tdicdcs	Tdicdcs – 1.24	Tdicdcs	Tdicdcs+1.24	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2]Display interface clock period value for read

$$Tdicpr = T_{DI_CLK} \times ceil\left[\frac{DISP\#_IF_CLK_PER_RD}{DI_CLK_PERIOD}\right]$$

[3]Display interface clock period value for write

$$Tdicpw = T_{DI_CLK} \times ceil\left[\frac{DISP\#_IF_CLK_PER_WR}{DI_CLK_PERIOD}\right]$$

[4]Display interface clock down time for read

$$Tdicdr = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

[5]Display interface clock up time for read

$$Tdicur = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

[6]Display interface clock down time for write

$$Tdicdw = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

[7]Display interface clock up time for write

$$Tdicuw = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

[8]This parameter is a requirement to the display connected to the IPU.

[9]Data read point

$$Tdrp = T_{DI_CLK} \times ceil\left[\frac{DISP_READ_EN}{DI_CLK_PERIOD}\right]$$

DISP_RD_EN is predefined in REGISTER.

[10]Loop back delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a chip-level output delay, board delays, a chip-level input delay, an IPU input delay. This value is chip specific.

[11]Display interface clock offset value

$$Toclk = T_{DI_CLK} \times ceil\left[\frac{DISP_CLK_OFFSET}{DI_CLK_PERIOD}\right]$$

CLK_OFFSET is predefined in REGISTER.

[12]Display RS up time

$$Tdicurs = T_{DI_CLK} \times ceil\left[\frac{DISP_RS_UP_\#}{DI_CLK_PERIOD}\right]$$

DISP_RS_UP is predefined in REGISTER.

[13]Display RS down time

$$Tdicdrs = T_{DI_CLK} \times ceil\left[\frac{DISP_RS_DOWN_\#}{DI_CLK_PERIOD}\right]$$

DISP_RS_DOWN is predefined in REGISTER.

[14]Display RS up time

$$Tdicucs = T_{DI_CLK} \times ceil\left[\frac{DISP_CS_UP_\#}{DI_CLK_PERIOD}\right]$$

DISP_CS_UP is predefined in REGISTER.

[15]Display RS down time

$$Tdicdcs = (T_{DI_CLK} \times ceil)\left[\frac{DISP_CS_DOWN_\#}{DI_CLK_PERIOD}\right]$$

DISP_CS_DOWN is predefined in REGISTER.

4.7.9 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits”.

4.7.10 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB Controller module.

Figure 60 and Figure 61 show the timing of MediaLB Controller, and Table 63 and Table 64 lists the MediaLB controller timing characteristics.

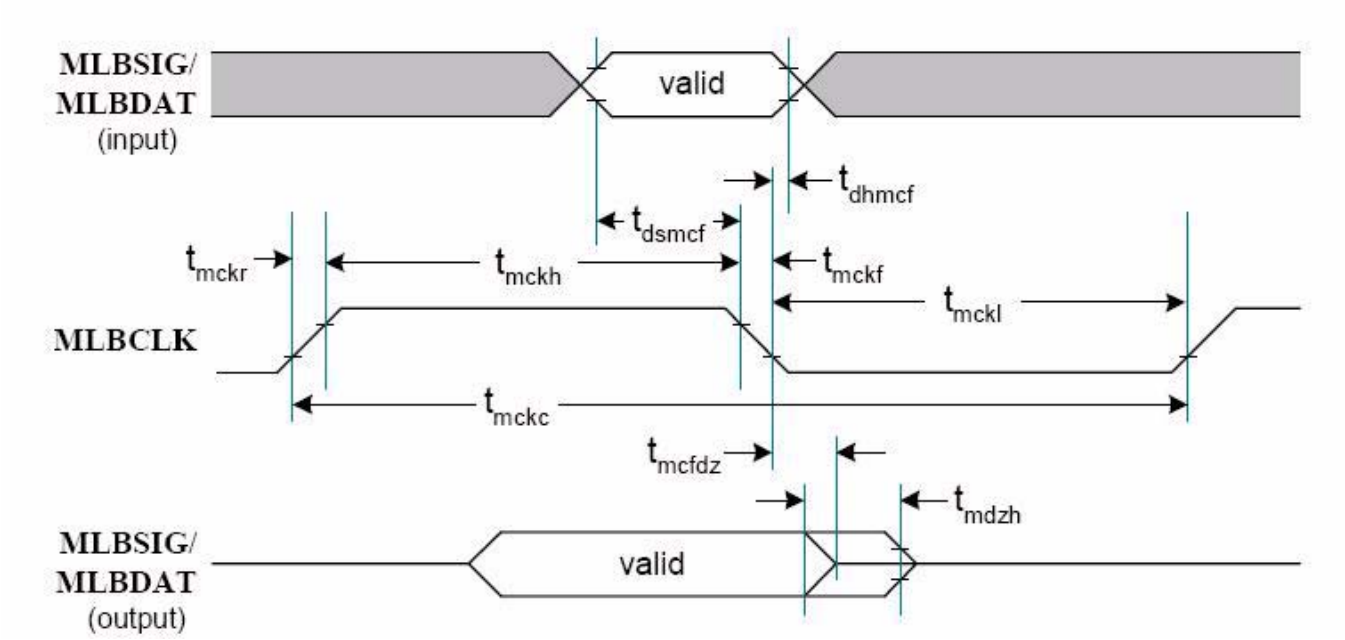


Figure 60. MediaLB Timing

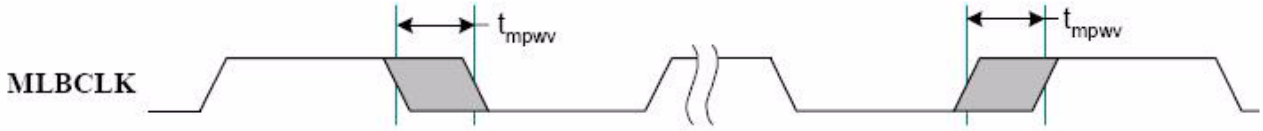


Figure 61. MediaLB Pulse Width Variation Timing

Ground = 0.0 V; Load Capacitance = 60 pF; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 63. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	12.288 24.576	24.6272 25.600	MHz	Min: 256*fs at 44.0 kHz Typ: 256*fs at 48.0 kHz Typ: 512*fs at 48.0 kHz Max: 512*fs at 48.1 kHz Max: 512*fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} TO V_{IH}
MLB fall time	t_{mckf}	—	—	3	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	— —	81 40	— —	ns	256*Fs 512*Fs
MLBCLK low time	t_{mckl}	31.5 30	37 35.5	— —	ns	256*Fs 256*Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512*Fs 512*Fs PLL unlocked
MLBCLK high time	t_{mckh}	31.5 30	38 36.5	— —	ns	256*Fs 256*Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512*Fs 512*Fs PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	2	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	4	—	—	ns	Note[3]

1 The MLB controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in Table 64; unless otherwise noted.

Table 64. MLB Device 1024 Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056	49.152	49.2544 51.200	MHz	Min: 1024*fs at 44.0 kHz Typ: 1024*fs at 48.0 kHz Max: 1024fs*fs at 48.1 kHz Max: 1024*fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	1	ns	V_{IL} TO V_{IH}
MLB fall time	t_{mckf}	—	—	1	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	—	20.3	—	ns	—
MLBCLK low time	t_{mckl}	6.5 6.1	7.7 7.3	—	ns	 PLL unlocked
MLBCLK high time	t_{mckh}	9.7 9.3	10.6 10.2	— —	ns	 PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	0.7	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	2	—	—	ns	Note[3]

1 The MLB Controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

4.7.11 One-Wire (OWIRE) Timing Parameters

Figure 62 depicts the RPP timing, and Table 65 lists the RPP timing parameters.

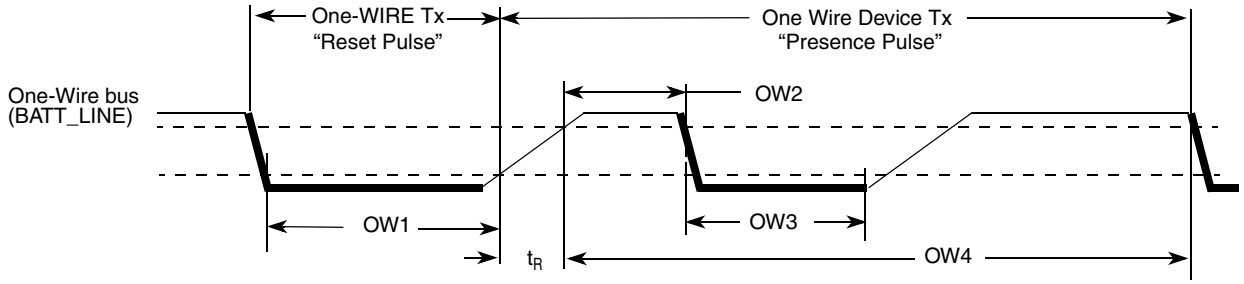


Figure 62. Reset and Presence Pulses (RPP) Timing Diagram

Table 65. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Unit
OW1	Reset Time Low	t_{RSTL}	480	511	—[1]	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High (includes recovery time)	t_{RSTH}	480	512	—	µs

[1] In order not to mask signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs.

Figure 63 depicts Write 0 Sequence timing, and Table 66 lists the timing parameters.

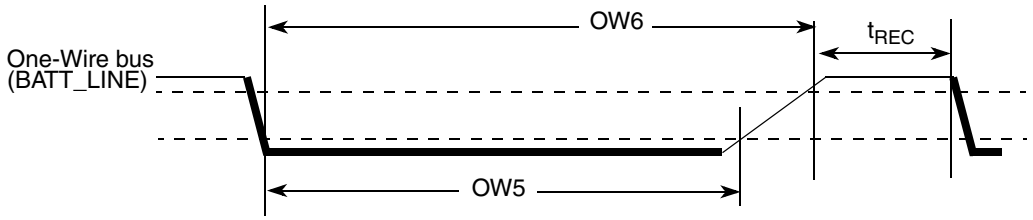


Figure 63. Write 0 Sequence Timing Diagram

Table 66. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW5	Write 0 Low Time	t_{LOW0}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs
	Recovery time	t_{REC}	1	—	—	µs

Figure 64 depicts Write 1 Sequence timing, Figure 65 depicts the Read Sequence timing, and Table 67 lists the timing parameters.

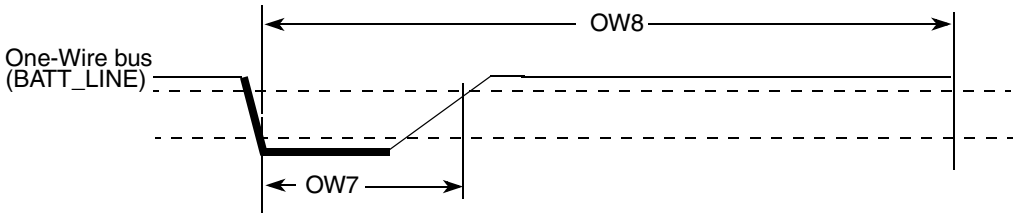


Figure 64. Write 1 Sequence Timing Diagram

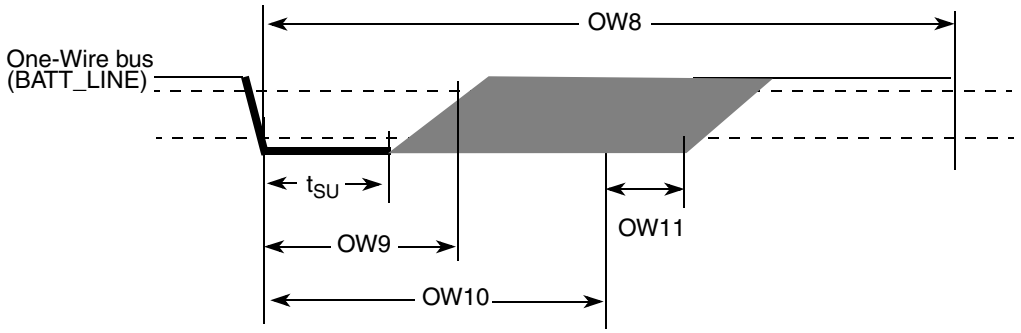


Figure 65. Read Sequence Timing Diagram

Table 67. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW7	Write 1 Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
	Read Data Setup	t_{SU}	—	—	1	µs
OW9	Read Low Time	t_{LOWR}	1	5	15	µs
OW10	Read Data Valid	t_{RDV}	—	15	—	µs
OW11	Release Time	$t_{RELEASE}$	0	—	45	µs

4.7.12 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 66 depicts the timing of the PWM, and Table 68 lists the PWM timing parameters.

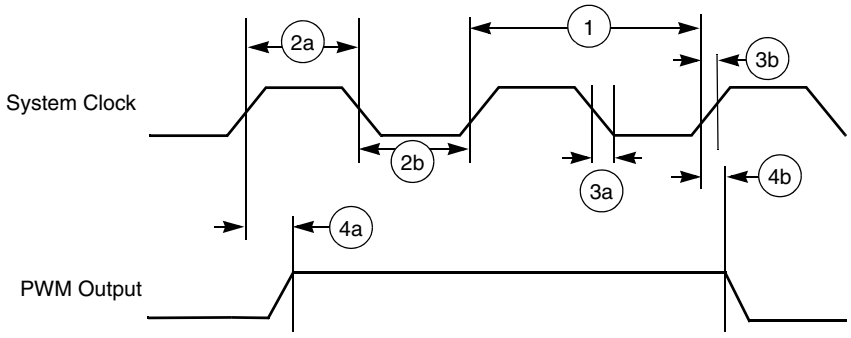


Figure 66. PWM Timing

Table 68. PWM Output Timing Parameter

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

1 CL of PWMO = 30 pF

4.7.13 PATA Timing Parameters

This section describes the timing parameters of the Parallel ATA module which are compliant with ATA/ATAPI-6 specification.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100MB/s. Parallel ATA module interface consist of a total of 29 pins. Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-6 specification and these requirements are configurable by the ATA module registers.

Table 69 and Figure 67 define the AC characteristics of all the PATA interface signals in all data transfer modes.

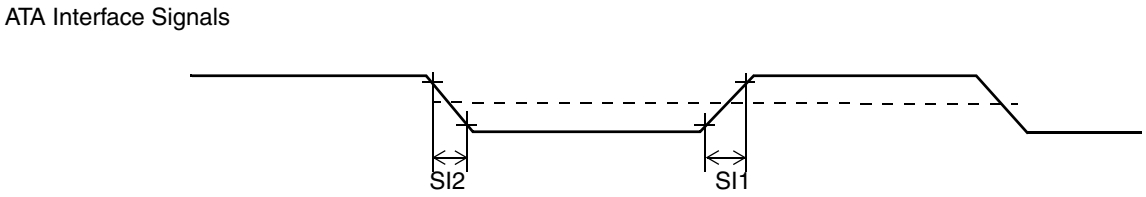


Figure 67. PATA Interface Signals Timing Diagram

Table 69. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min	Max	Unit
SI1	Rising edge slew rate for any signal on ATA interface[1]	S_{rise}	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on ATA interface[1]	S_{fall}	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

1 SRISE and SFALL shall meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15–40 pF where all signals have the same capacitive load value.

The user must use level shifters for 5.0 V compatibility on the ATA interface. The i.MX53xA PATA interface is 3.3 V compatible.

The use of bus buffers introduces delay on the bus and skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX53xA PATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 70 shows ATA timing parameters.

Table 70. PATA Timing Parameters

Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (AHB_CLK_ROOT)	Peripheral clock frequency (7.5 ns for 133 MHz clock)
ti_ds	Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time ata_data to bus clock L-to-H	8.5 ns
tsui	Set-up time ata_iordy to bus clock H-to-L	8.5 ns
thi	Hold time ata_iordy to bus clock H to L	2.5 ns
tskew1	Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	7 ns
tskew2	Max difference in buffer propagation delay for any of following signals: ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	Transceiver
tskew3	Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read)	Transceiver

Table 70. PATA Timing Parameters (continued)

Name	Description	Value/ Contributing Factor[1]
tbuf	Max buffer propagation delay	Transceiver
tcable1	Cable propagation delay for ata_data	Cable
tcable2	Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack	Cable
tskew4	Max difference in cable propagation delay between ata_iordy and ata_data (read)	Cable
tskew5	Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)	Cable
tskew6	Max difference in cable propagation delay without accounting for ground bounce	Cable

1 Values provided where applicable.

4.7.13.1 PIO Mode Read Timing

Figure 68 shows timing for PIO read. Table 71 lists the timing parameters for PIO read.

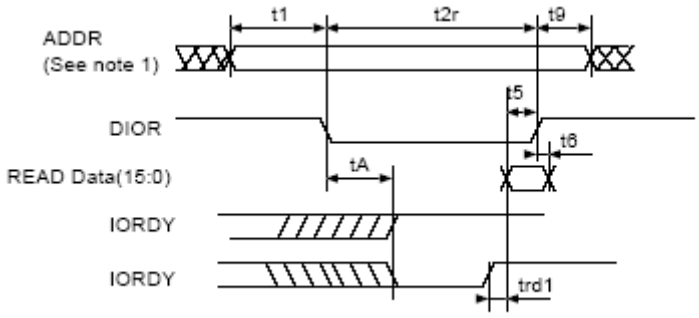


Figure 68. PIO Read Timing Diagram

Table 71. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 68	Value	Controlling Variable
t1	t1	t1(min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2 (read)	t2r	t2(min) = time_2r * T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9(min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_9
t5	t5	t5(min) = tco + tsu + tbuf + tbuf+ tcable1 + tcable2	time_2 (affects tsu and tco)
t6	t6	0	—
tA	tA	tA(min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
trd	trd1	trd1(max) = (–trd)+ (tskew3 + tskew4) trd1(min) = (time_pio_rdx – 0.5)*T – (tsu + thi) (time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0(min) = (time_1 + time_2r+ time_9) * T	time_1, time_2r, time_9

Figure 69 shows timing for PIO write. Table 72 lists the timing parameters for PIO write.

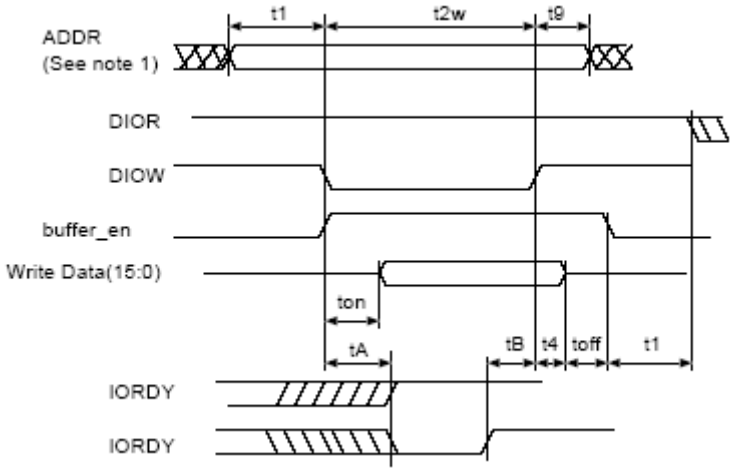


Figure 69. Multi-word DMA (MDMA) Timing

Table 72. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 69	Value	Controlling Variable
t1	t1	t1(min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2 (write)	t2w	t2(min) = time_2w * T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9(min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3(min) = (time_2w – time_on)* T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4(min) = time_4 * T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough	—
—	—	Avoid bus contention when switching buffer off by making toff long enough	—

Figure 70 shows timing for MDMA read, Figure 71 shows timing for MDMA write, and Table 73 lists the timing parameters for MDMA read and write.

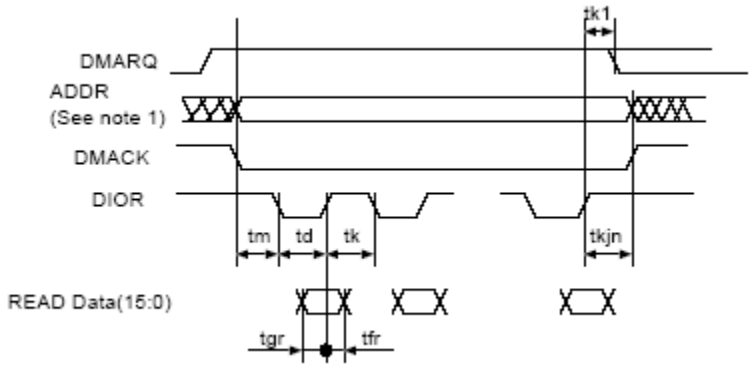


Figure 70. MDMA Read Timing Diagram

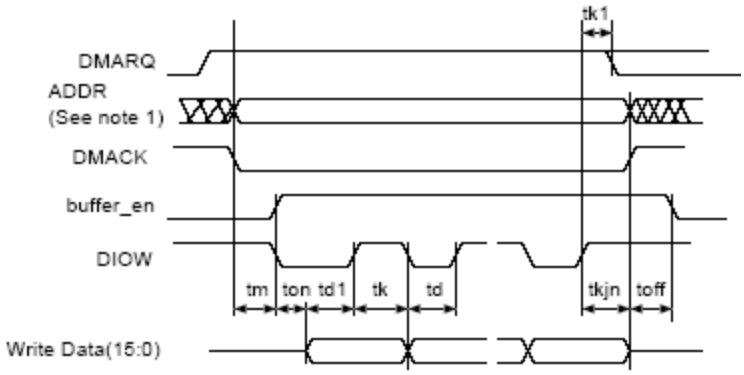


Figure 71. MDMA Write Timing Diagram

Table 73. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 70 (Read), Figure 71 (Write)	Value	Controlling Variable
tm, ti	tm	tm(min) = ti(min) = time_m * T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1(min) = td(min) = time_d * T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk[1]	tk(min) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0(min) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr(min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr(min) = 5 ns	—
tg(write)	—	tg(min-write) = time_d * T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf(min-write) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k – 2)×T – (tsu + tco + 2×tbuf + 2×tcable2)	time_d, time_k[2]

Table 73. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 70 (Read), Figure 71 (Write)	Value	Controlling Variable
tn, tj	tkjn	tn= tj= tkjn = time_jn * T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 tk1 in the MDMA figures (**Figure 70** and **Figure 71**) equals (tk – 2*T).

2 tk1 in the MDMA figures equals (tk – 2*T).

4.7.13.2 Ultra DMA (UDMA) Input Timing

Figure 72 shows timing when the UDMA in transfer starts, Figure 73 shows timing when the UDMA in host terminates transfer, Figure 74 shows timing when the UDMA in device terminates transfer, and Table 74 lists the timing parameters for UDMA in burst.

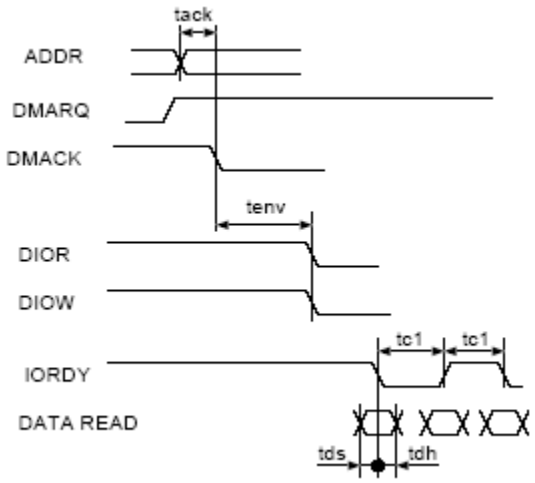


Figure 72. UDMA in Transfer Starts Timing Diagram

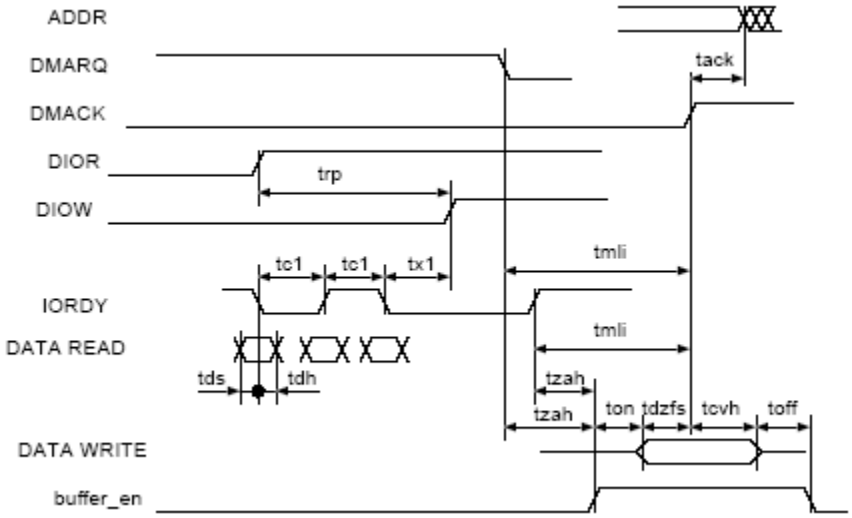


Figure 73. UDMA in Host Terminates Transfer Timing Diagram

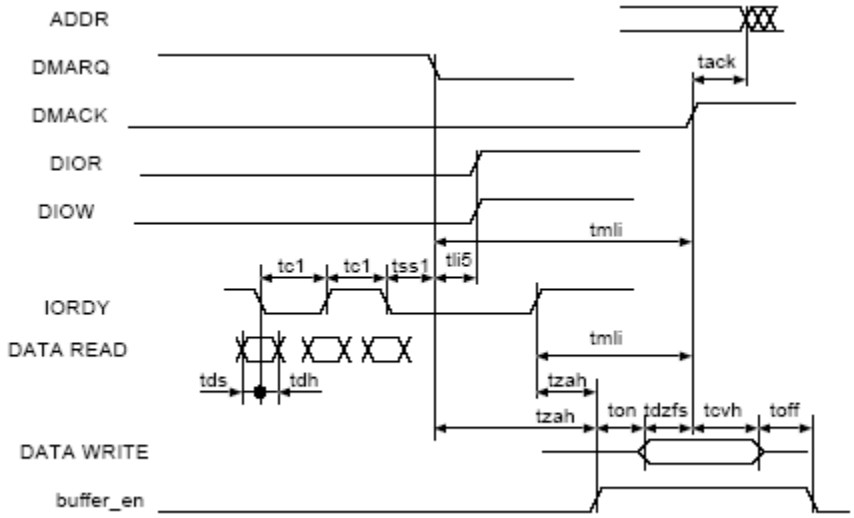


Figure 74. UDMA in Device Terminates Transfer Timing Diagram

Table 74. UDMA in Burst Timing Parameters

ATA Parameter	Parameter from Figure 72, Figure 73, Figure 74	Description	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	

Table 74. UDMA in Burst Timing Parameters (continued)

ATA Parameter	Parameter from Figure 72, Figure 73, Figure 74	Description	Controlling Variable
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 ×tbuf + 2×tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff[2]	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2 Make ton and toff big enough to avoid bus contention.

4.7.13.3 UDMA Output Timing

Figure 75 shows timing when the UDMA out transfer starts, Figure 76 shows timing when the UDMA out host terminates transfer, Figure 77 shows timing when the UDMA out device terminates transfer, and Table 75 lists the timing parameters for UDMA out burst.

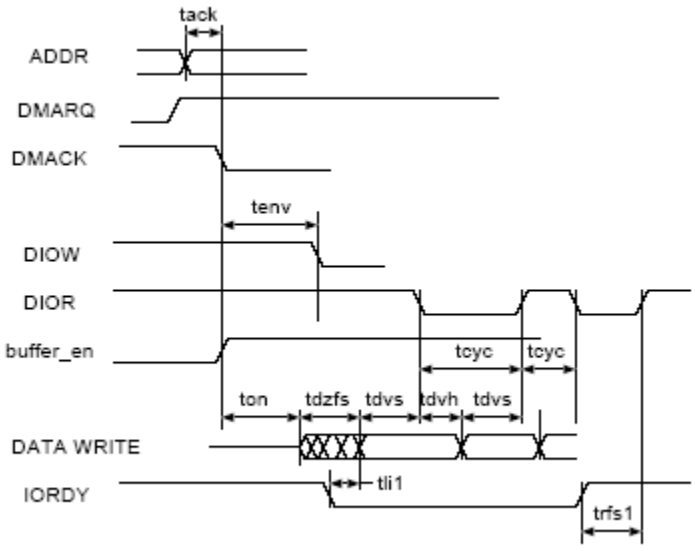


Figure 75. UDMA Out Transfer Starts Timing Diagram

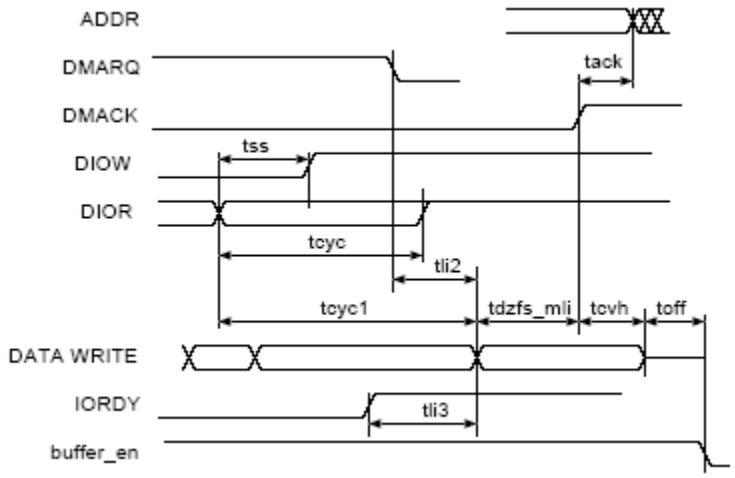


Figure 76. UDMA Out Host Terminates Transfer Timing Diagram

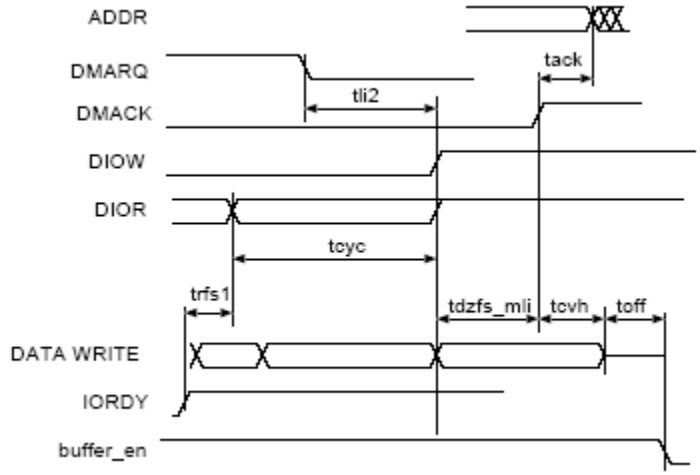


Figure 77. UDMA Out Device Terminates Transfer Timing Diagram

Table 75. UDMA Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 75, Figure 76, Figure 77	Value	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs × T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc

Table 75. UDMA Out Burst Timing Parameters (continued)

ATA Parameter	Parameter from Figure 75, Figure 76, Figure 77	Value	Controlling Variable
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max (time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.7.14 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.7.14.1 Reference Clock Electrical and Jitter Specifications

The refclk signal is differential and supports frequencies of 25 MHz or 50-156.25 MHz (100 MHz and 125 MHz are common frequencies). The frequency is pin-selectable (for more information about the signal, see “Per-Transceiver Control and Status Signals” in the SATA PHY chapter in the Reference Manual).

Table 76 provides the SATA PHY reference clock specifications.

Table 76. Reference Clock Specifications

Parameters	Test Conditions	Min	Max	Unit
Differential peak voltage (typically 0.71 V)	—	350	850	mV
Common mode voltage (refclk_p + refclk_m) / 2	—	175	2,000	mV
Total phase jitter	For information about total phase jitter, see following section	—	3	ps RMS
Minimum/maximum duty cycle	—	40	60	% UI
Frequency range	—	25	156.25	MHz

4.7.14.1.1 Reference Clock Jitter Measurement

The total phase jitter on the reference clock is specified at 3 ps RMS. There are numerous ways to measure the reference clock jitter, one of which is as follows.

Using a high-speed sampling scope (20 GSamples/s), 1 million samples of the differential reference clock are taken, and the zero-crossing times of each rising edge are calculated. From the zero-crossing data, an average reference clock period is calculated. This average reference clock period is subtracted from each sequential, instantaneous period to find the difference between each reference clock rising edge and the ideal placement to produce the phase jitter sequence. The power spectral density (PSD) of the phase jitter is calculated and integrated after being weighted with the transfer function shown in Figure 78. The square root of the resultant integral is the RMS total phase jitter.

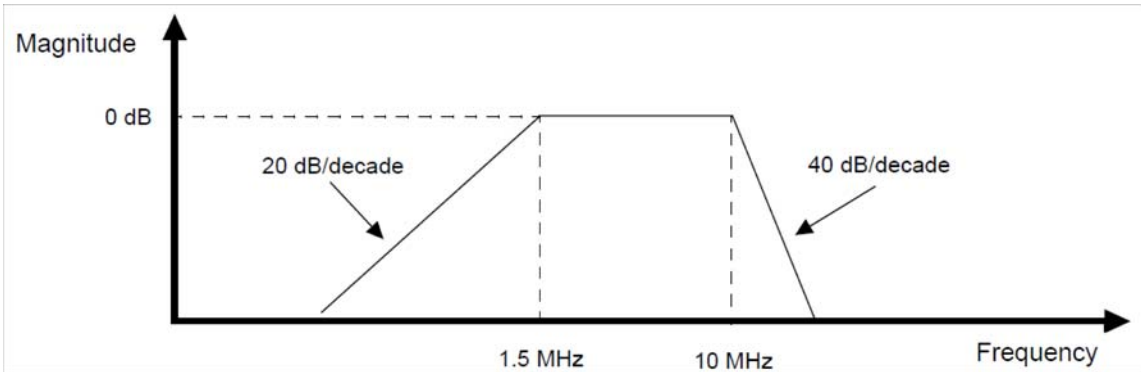


Figure 78. Weighting Function for RMS Phase Jitter Calculation

4.7.14.2 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specification. The following subsections provide values obtained from a combination of simulations and silicon characterization.

NOTE

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

4.7.14.2.1 SATA PHY Transmitter Characteristics

Table 77 provides specifications for SATA PHY transmitter characteristics.

Table 77. SATA2 PHY Transmitter Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Transmit common mode voltage	V_{CTM}	0.4	—	0.6	V
Transmitter pre-emphasis accuracy (measured change in de-emphasized bit)	—	–0.5	—	0.5	dB

4.7.14.2.2 SATA PHY Receiver Characteristics

Table 78 provides specifications for SATA PHY receiver characteristics.

Table 78. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN_RX_EYE_HEIGHT}$	—	—	175	mV
Tolerance	PPM	–400	—	400	ppm

4.7.14.3 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.7.14.4 SATA Connectivity When Not in Use

NOTE

The Temperature Sensor is part of the SATA module. If SATA IP is disabled, the Temperature Sensor will not work as well. Temperature Sensor functionality is important in supporting high performance applications without overheating the device (at high ambient temp).

When both SATA and thermal sensor are not required, connect VP and VPH supplies to ground. The rest of the ports, both inputs and outputs (SATA_REFCLKM, SATA_REFCLKP, SATA_REXT, SATA_RXM, SATA_RXP, SATA_TXM) can be left floating. It is not recommended to turn off the VPH while the VP is active.

When SATA is not in use but thermal sensor is still required, both VP and VPH supplies must be powered on according to their nominal voltage levels. The reference clock input frequency must fall within the specified range of 25 MHz to 156.25 MHz. SATA_REXT does not need to be connected, as the termination impedance is not of consequence.

4.7.15 SCAN JTAG Controller (SJC) Timing Parameters

Figure 79 depicts the SJC test clock input timing. Figure 80 depicts the SJC boundary scan timing. Figure 81 depicts the SJC test access port. Signal parameters are listed in Table 79.

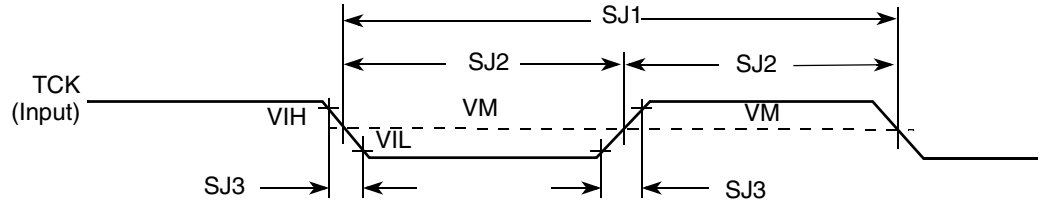


Figure 79. Test Clock Input Timing Diagram

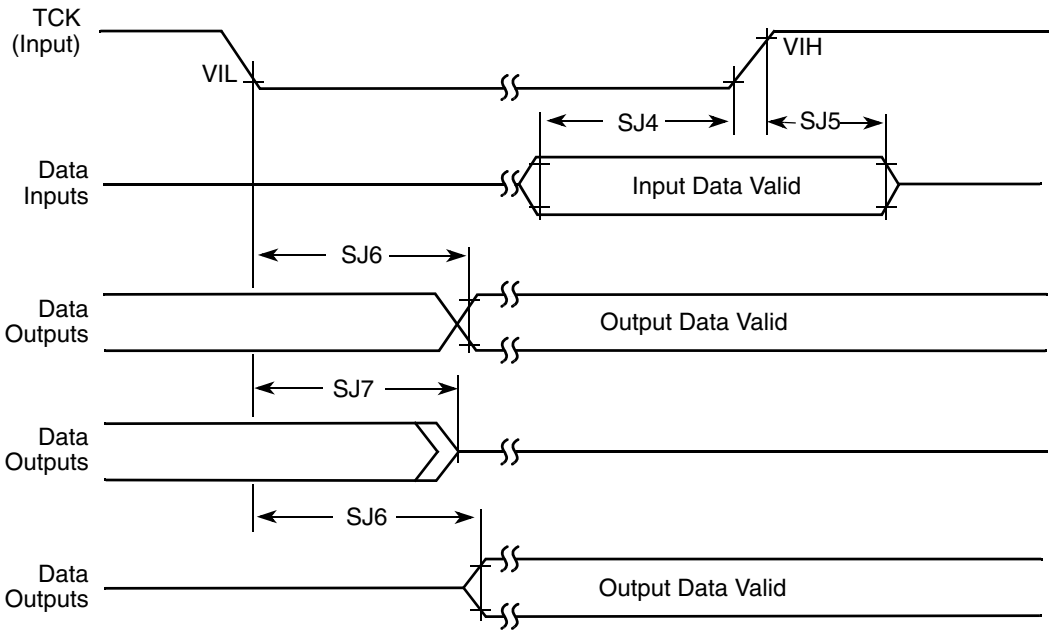


Figure 80. Boundary Scan (JTAG) Timing Diagram

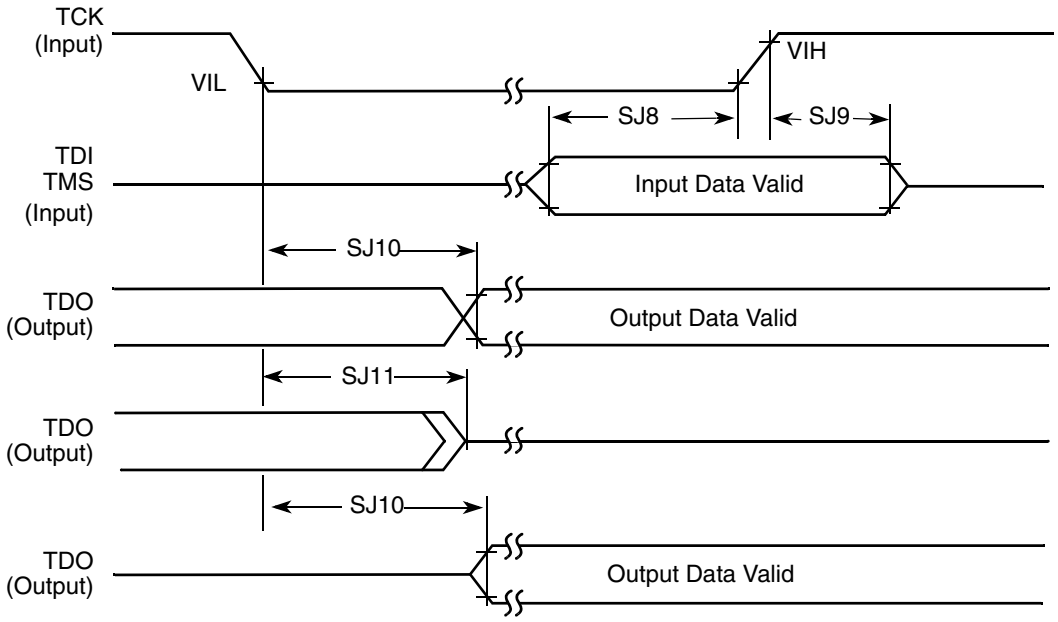


Figure 81. Test Access Port Timing Diagram

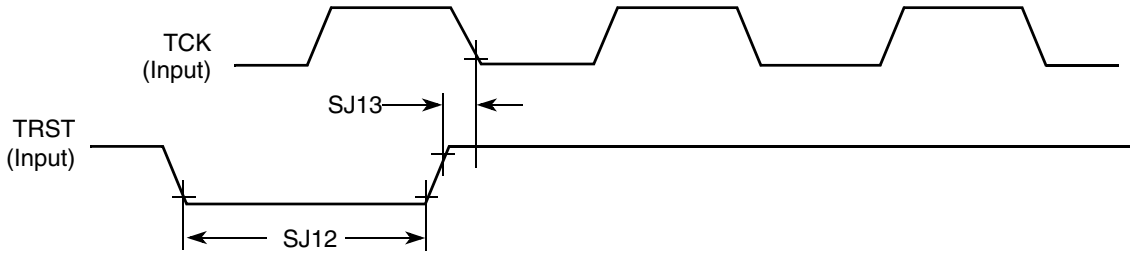


Figure 82. $\overline{\text{TRST}}$ Timing Diagram

Table 79. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns

Table 79. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.7.16 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 80 shows SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 80. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Units
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

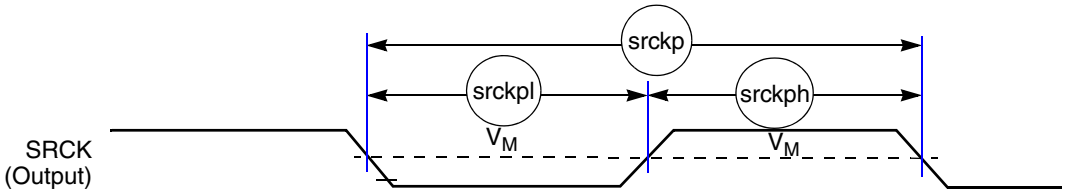


Figure 83. SPDIF Timing Diagram

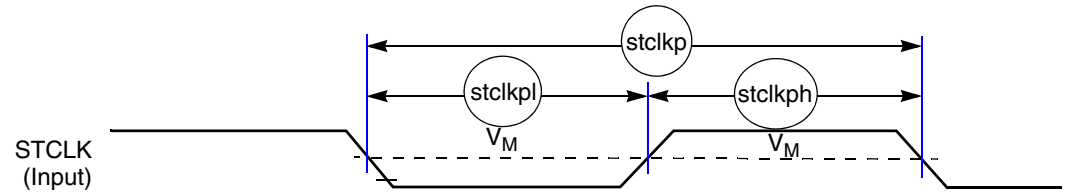


Figure 84. STCLK Timing

4.7.17 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 81.

Table 81. AUDMUX Port Allocation

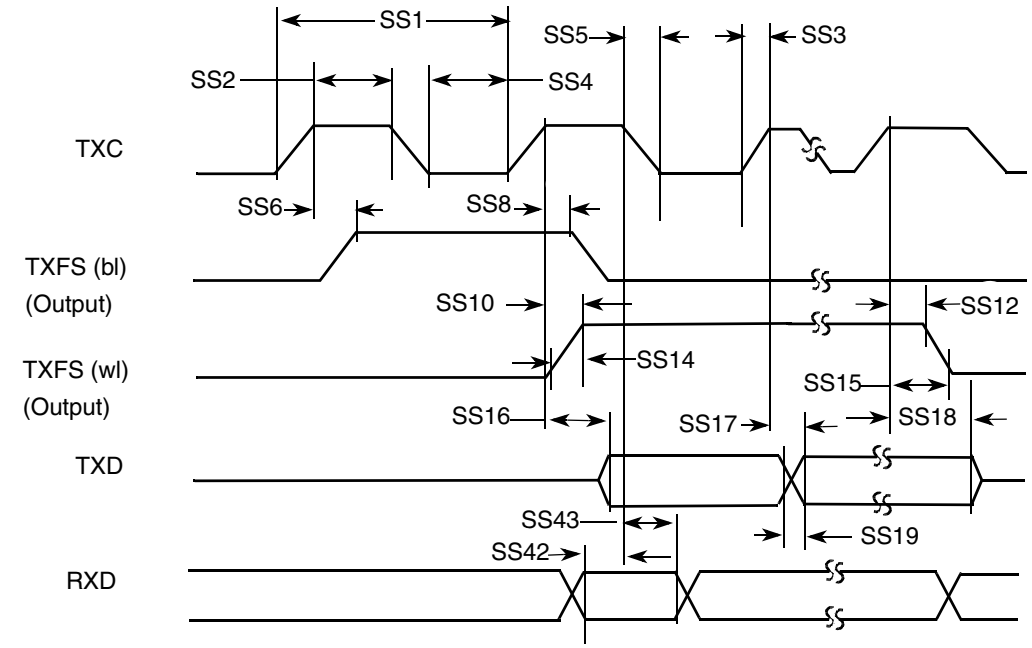
Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External – EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the i.MX53 reference manual are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.7.17.1 SSI Transmitter Timing with Internal Clock

Figure 85 depicts the SSI transmitter internal clock timing and Table 82 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 85. SSI Transmitter Internal Clock Timing Diagram

Table 82. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns

Table 82. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6.0	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns
SS52	Loading	—	25.0	pF

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.17.2 SSI Receiver Timing with Internal Clock

Figure 86 depicts the SSI receiver internal clock timing and Table 83 lists the timing parameters for the receiver timing with the internal clock

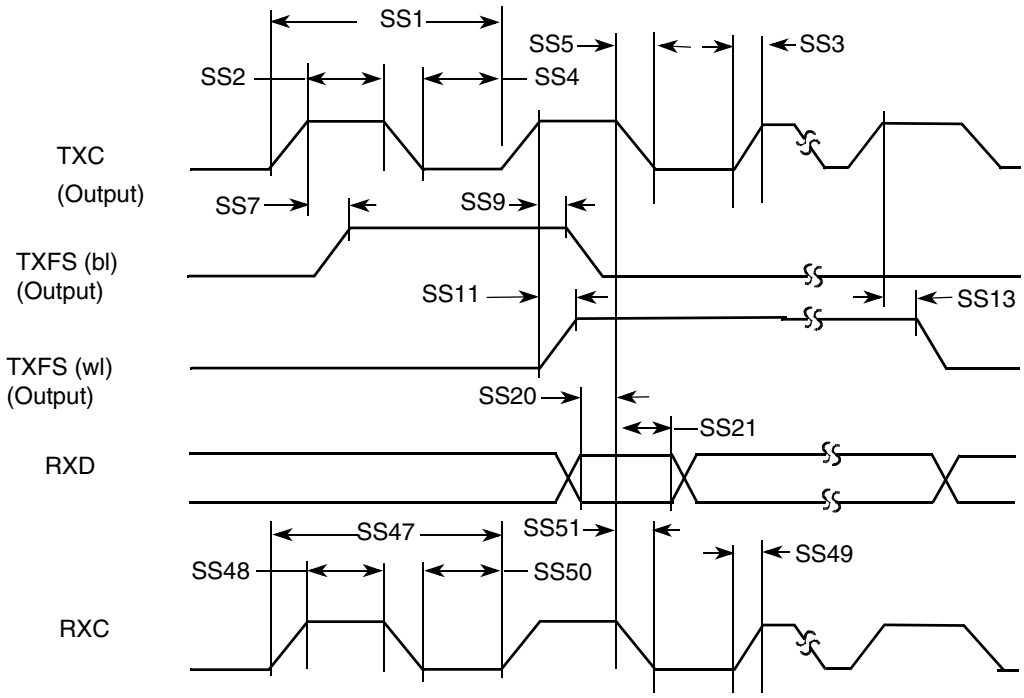


Figure 86. SSI Receiver Internal Clock Timing Diagram

Table 83. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns

Table 83. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.17.3 SSI Transmitter Timing with External Clock

Figure 87 depicts the SSI transmitter external clock timing and Table 84 lists the timing parameters for the transmitter timing with the external clock

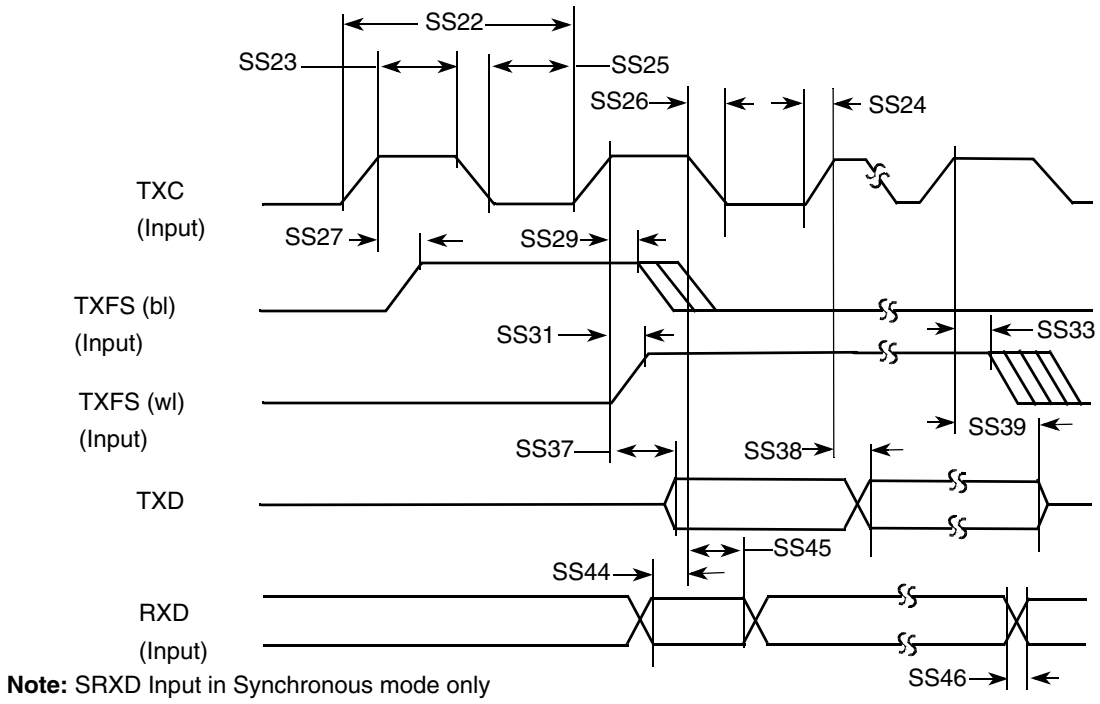


Figure 87. SSI Transmitter External Clock Timing Diagram

Table 84. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

Table 84. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.17.4 SSI Receiver Timing with External Clock

Figure 88 depicts the SSI receiver external clock timing and Table 85 lists the timing parameters for the receiver timing with the external clock.

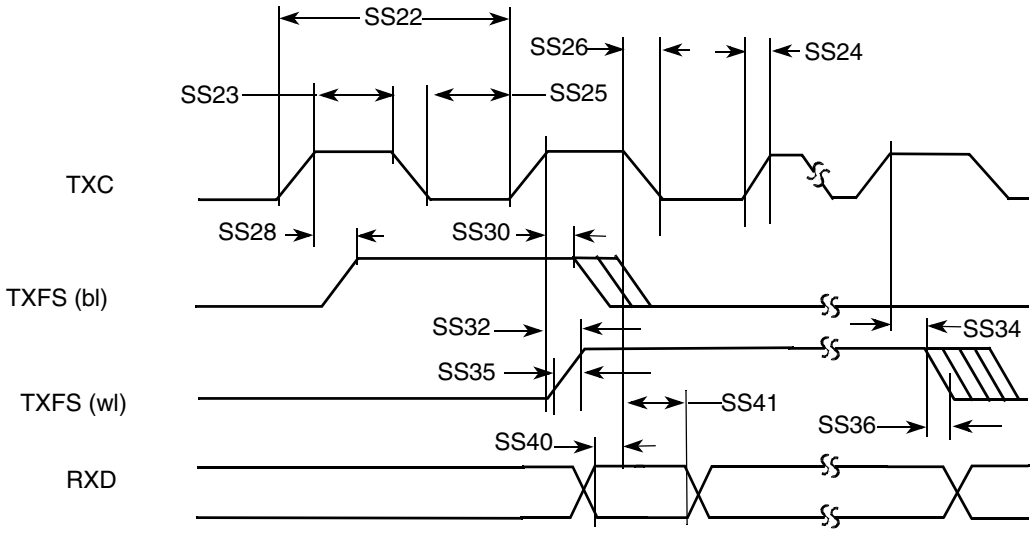


Figure 88. SSI Receiver External Clock Timing Diagram

Table 85. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	–10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.18 UART I/O Configuration and Timing Parameters

4.7.18.1 UART RS-232 I/O Configuration in Different Modes

The i.MX53xA UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 86 shows the UART I/O configuration based on the enabled mode.

Table 86. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.7.18.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.7.18.2.1 UART Transmitter

Figure 89 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 87 lists the UART RS-232 serial mode transmit timing characteristics.

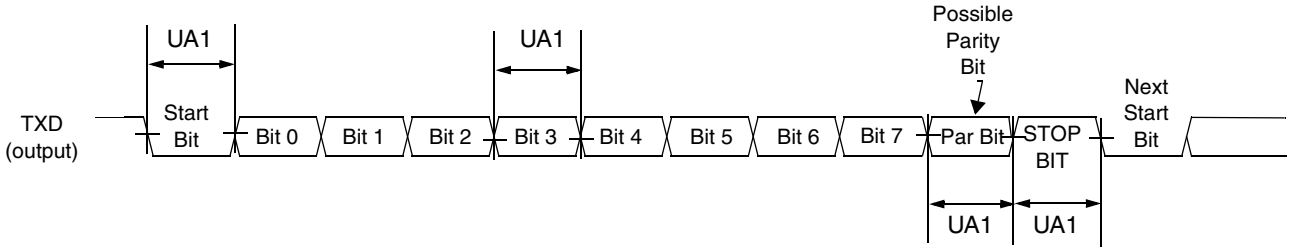


Figure 89. UART RS-232 Serial Mode Transmit Timing Diagram

Table 87. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud_rate}$ + T_{ref_clk}	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.7.18.2.2 UART Receiver

Figure 90 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 88 lists serial mode receive timing characteristics.

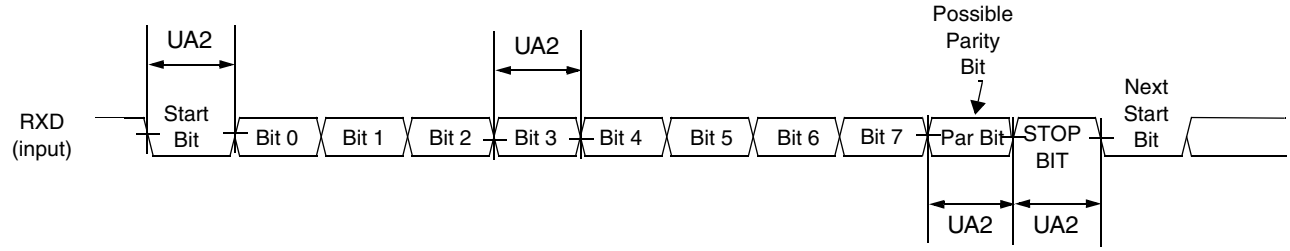


Figure 90. UART RS-232 Serial Mode Receive Timing Diagram

Table 88. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud_rate}$ [2] – $1/(16*F_{baud_rate})$	$1/F_{baud_rate}$ + $1/(16*F_{baud_rate})$	—

[1] The UART receiver can tolerate $1/(16*F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.7.18.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.7.18.3.3 UART IrDA Mode Transmitter

Figure 91 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 89 lists the transmit timing characteristics.

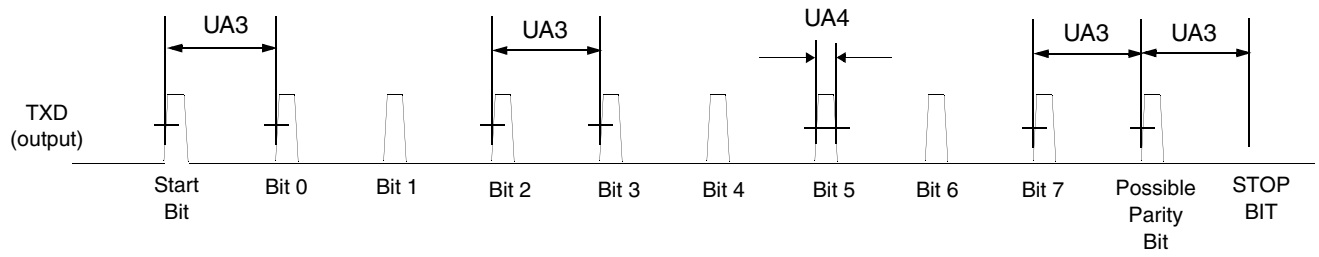


Figure 91. UART IrDA Mode Transmit Timing Diagram

Table 89. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud_rate} + T_{ref_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud_rate}) - T_{ref_clk}$	$(3/16)*(1/F_{baud_rate}) + T_{ref_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.7.18.3.4 UART IrDA Mode Receiver

Figure 92 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 90 lists the receive timing characteristics.

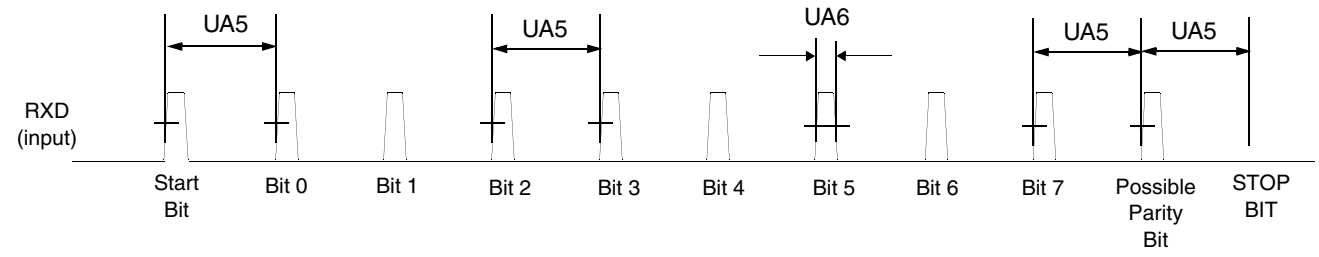


Figure 92. UART IrDA Mode Receive Timing Diagram

Table 90. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud_rate}$[2] – $1/(16*F_{baud_rate})$	$1/F_{baud_rate} + 1/(16*F_{baud_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 us	$(5/16)*(1/F_{baud_rate})$	—

[1] The UART receiver can tolerate 1/(16*F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16*F_{baud_rate}).

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.7.19 USB-OH-3 Parameters

This section describes the electrical parameters of the USB OTG port and USB HOST ports. For on-chip USB PHY parameters see Section 4.7.20, "USB PHY Parameters."

4.7.19.1 Serial Interface

In order to support four serial different interfaces, the USB serial transceiver can be configured to operate in one of four modes:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

4.7.19.1.1 DAT_SE0 Bidirectional Mode

Table 91. Signal Definitions - DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	TX data when USB_TXOE_B is low Differential RX data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 RX indicator when USB_TXOE_B is high

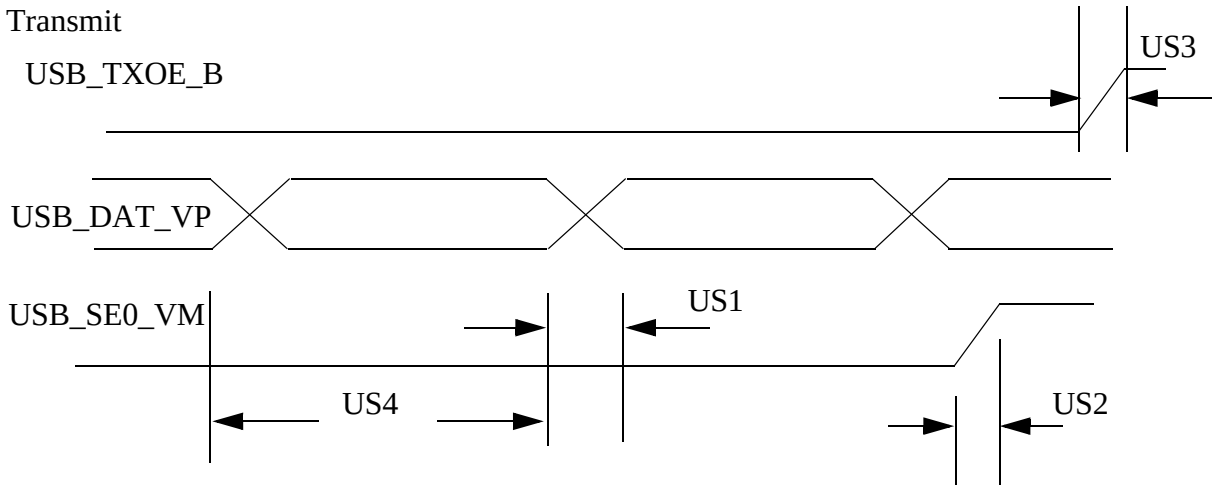


Figure 93. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

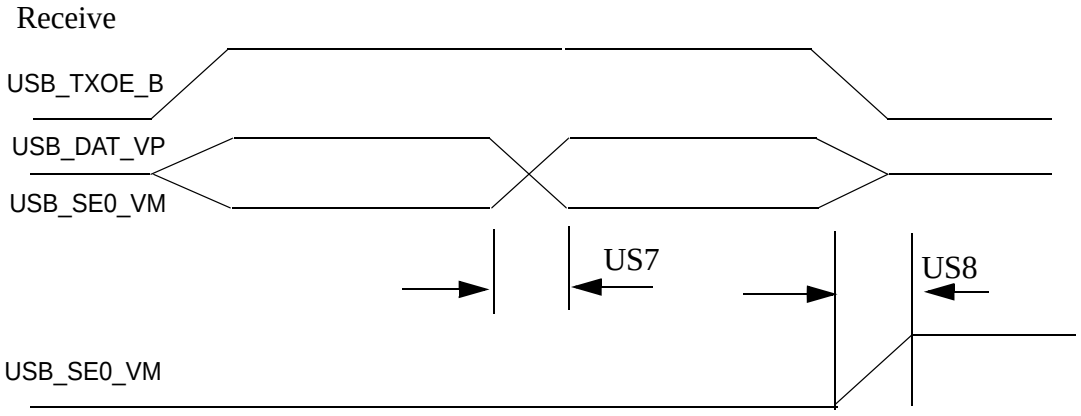


Figure 94. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 92. Definitions of USB Waveform in DAT_SE0 Bi-Directional Mode

No.	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions / Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	-—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.7.19.1.2 DAT_SE0 Unidirectional Mode

Table 93. Signal Definitions - DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	TX data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high

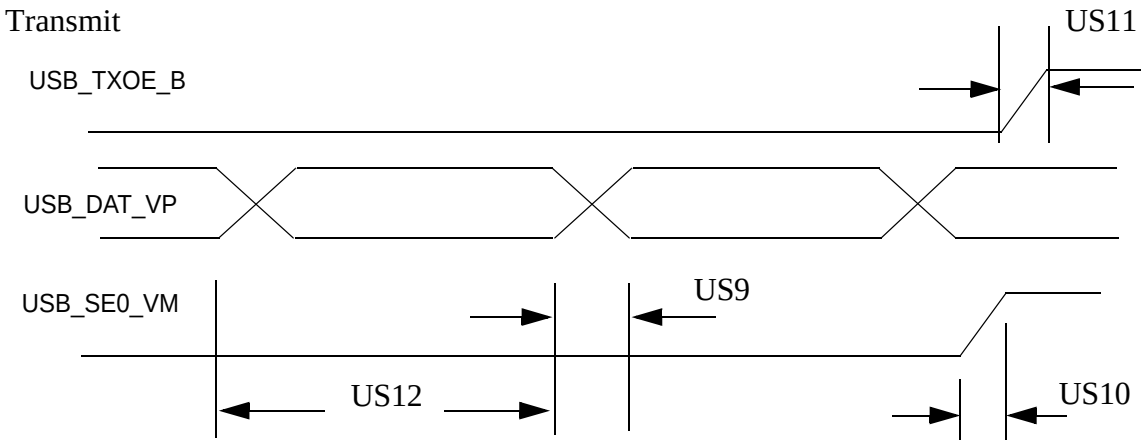


Figure 95. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

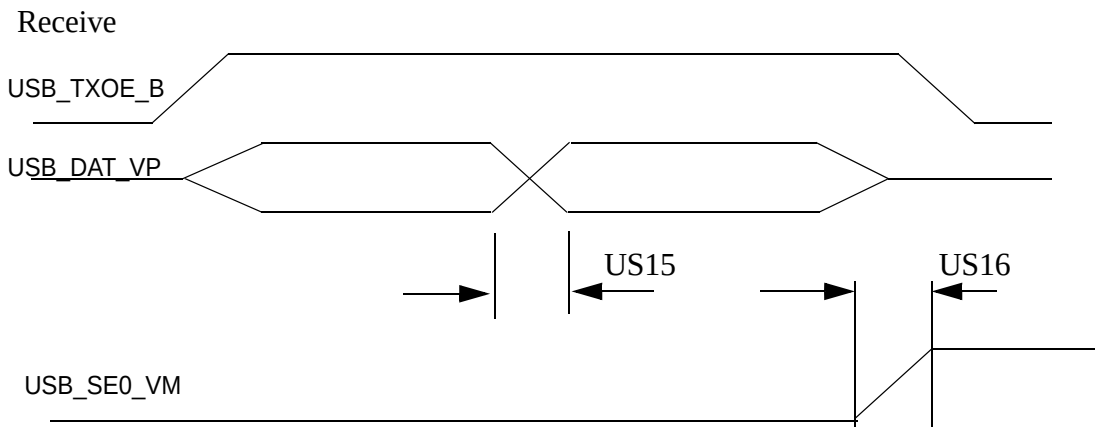


Figure 96. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 94. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

No.	Parameter	Signal Name	Signal Source	Min	Max	Unit	Condition / Reference Signal
US9	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US16	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF

4.7.19.1.3 VP_VM Bidirectional Mode

Table 95. Signal Definitions - VP_VM Bidirectional mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	TX VP data when USB_TXOE_B is low RX VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	TX VM data when USB_TXOE_B low RX VM data when USB_TXOE_B high

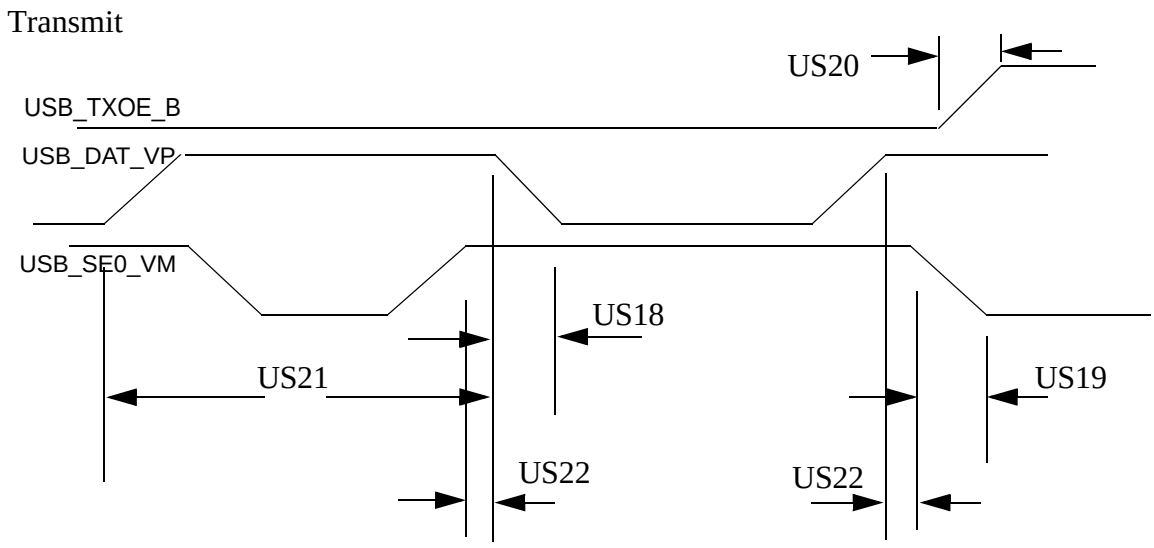


Figure 97. USB Transmit Waveform in VP_VM Bidirectional Mode

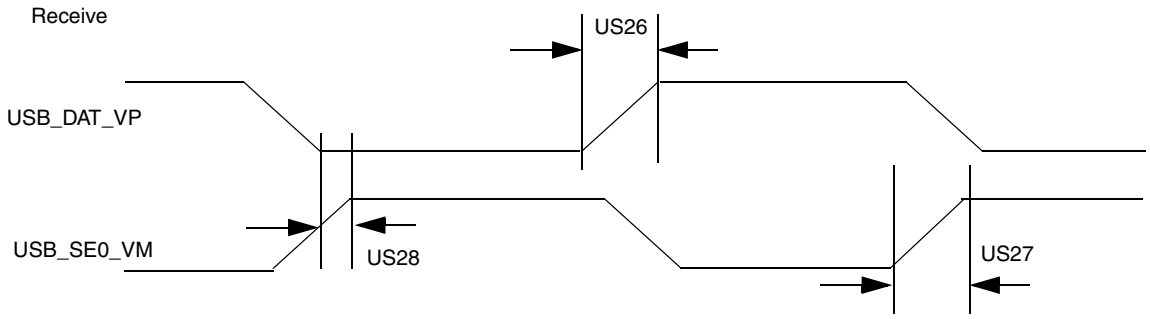


Figure 98. USB Receive Waveform in VP_VM Bidirectional Mode

Table 96. USB Port Timing Specification in VP_VM Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min	Max	Unit	Condition / Reference Signal
US18	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US19	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US20	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US21	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US22	TX Overlap	USB_SE0_VM	Out	-3.0	+3.0	ns	USB_DAT_VP
US26	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US27	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF
US28	RX Skew	USB_DAT_VP	In	-4.0	+4.0	ns	USB_SE0_VM

4.7.19.1.4 VP_VM Unidirectional Mode

Table 97. Signal Definitions - VP_VM Unidirectional mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	TX VP data when USB_TXOE_B is low
USB_SE0_VM	Out	TX VM data when USB_TXOE_B is low
USB_VP1	In	RX VP data when USB_TXOE_B is high
USB_VM1	In	RX VM data when USB_TXOE_B is high

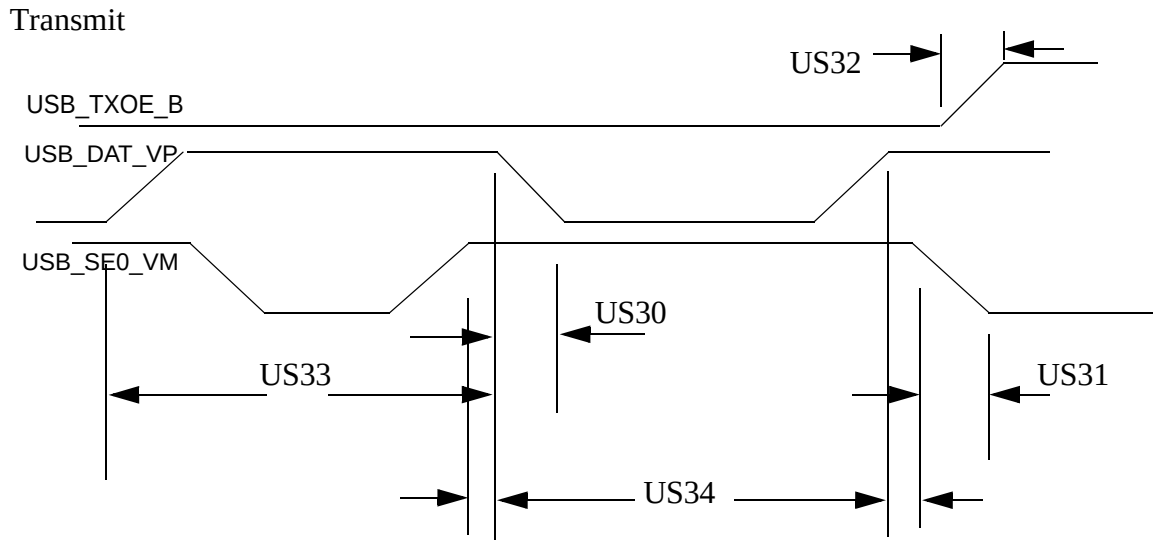


Figure 99. USB Transmit Waveform in VP_VM Unidirectional Mode

Receive

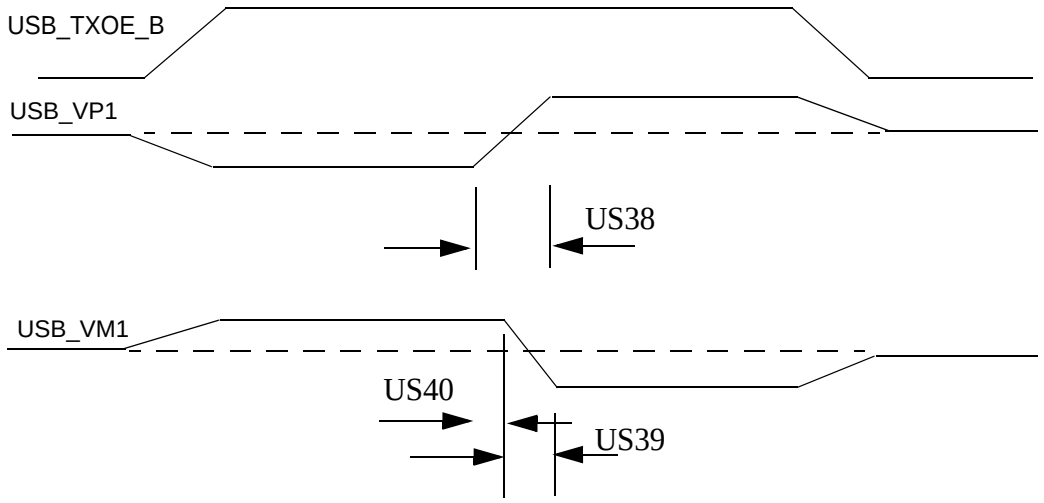


Figure 100. USB Receive Waveform in VP_VM Unidirectional Mode

Table 98. USB Timing Specification in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min	Max	Unit	Conditions / Reference Signal
US30	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	TX Overlap	USB_SE0_VM	Out	-3.0	3.0	ns	USB_DAT_VP
US38	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US39	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF
US40	RX Skew	USB_VP1	In	-4.0	+4.0	ns	USB_VM1

4.7.19.2 Parallel Interface (Normal ULPI) Timing

Electrical and timing specifications of Parallel Interface (Normal ULPI) for Host Port2 and Port3 are presented in the subsequent sections.

Table 99. Signal Definitions - Parallel Interface (Normal ULPI)

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to Clock.
USB_Data[7:0]	I/O	Bi-directional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the Data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

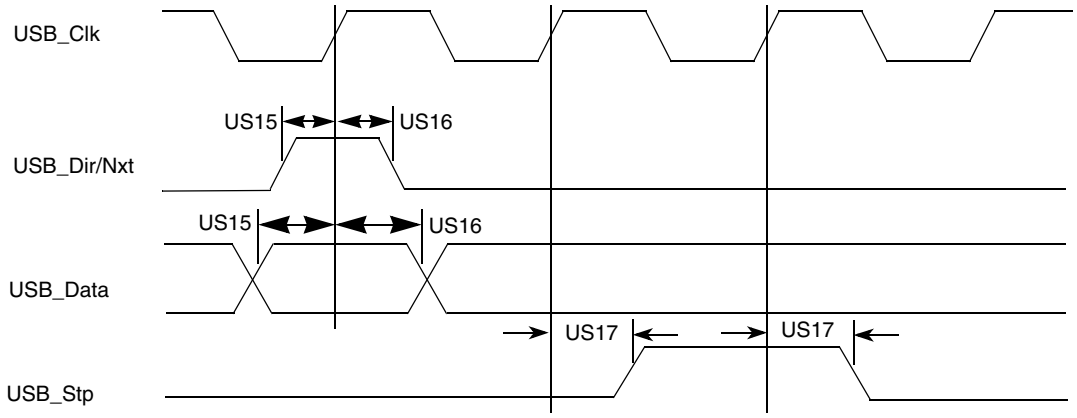


Figure 101. USB Transmit/Receive Waveform in Parallel Mode

Table 100. USB Timing Specification for Normal ULPI mode

ID	Parameter	Min	Max	Unit	Conditions / Reference Signal
US15	Setup Time(Dir&Nxt in, Data in)	—	6.0	ns	10 pF
US16	Hold Time(Dir&Nxt in, Data in)	—	0.0	ns	10 pF
US17	Output delay Time(Stp out, Data out	—	9.0	ns	10 pF

4.7.20 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

4.7.20.1 USB PHY AC Parameters

Table 101 lists the AC timing parameters for USB PHY.

Table 101. USB PHY AC Timing Parameters

Parameter	Conditions	Min	Typ	Max	Unit
trise	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	—	300 20	ns
tfall	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	—	300 20	ns
Jitter	1.5 Mbps 12 Mbps 480 Mbps	—	—	10 1 0.2	ns

4.7.20.2 USB PHY Additional Electrical Parameters

Table 102 lists the parameters for additional electrical characteristics for USB PHY.

Table 102. Additional Electrical Characteristics for USB PHY

Parameter	Conditions	Min	Typ	Max	Unit
Vcm DC (dc level measured at receiver connector)	HS Mode LS/FS Mode	–0.05 0.8	—	0.5 2.5	V
Crossover Voltage	LS Mode FS Mode	1.3 1.3	—	2 2	V
Power supply ripple noise (analog 3.3 V)	< 160 MHz	–50	0	50	mV
Power supply ripple noise (analog 2.5 V)	< 1.2 MHz > 1.2 MHz	–10 –50	0 0	10 50	mV
Power supply ripple noise (Digital 1.2 V)	All conditions	–50	0	50	mV

4.7.20.3 USB PHY System Clocking (SYSCLK)

Table 103 lists the USB PHY system clocking parameters.

Table 103. USB PHY System Clocking Parameters

Parameter	Conditions	Min	Typ	Max	Unit
Clock deviation	Reference Clock frequency 24 MHz	–150	—	150	ppm
Rise/fall time	—	—	—	200	ps
Jitter (peak-peak)	< 1.2 MHz	0	—	50	ps
Jitter (peak-peak)	> 1.2 MHz	0	—	100	ps
Duty-cycle	Reference Clock frequency 24 MHz	40	—	60	%

4.7.20.4 USB PHY Voltage Thresholds

Table 104 lists the USB PHY voltage thresholds.

Table 104. VBUS Comparators Thresholds

Parameter	Conditions	Min	Typ	Max	Unit
A-Device Session Valid	—	0.8	1.4	2.0	V
B-Device Session Valid	—	0.8	1.4	4.0	V
B-Device Session End	—	0.2	0.45	0.8	V
VBUS Valid Comparator Threshold[1]	—	4.4	4.6	4.75	V

1 For VBUS maximum rating, see Table 4 on page 18

4.7.20.5 USB PHY Termination

USB driver impedance in FS and HS modes is 45 Ω ±10% (steady state). No external resistors required.

4.8 XTAL and CKIL Electricals

Table 105 shows the XTALOSC electrical specifications.

Table 105. XTALOSC Electrical Specifications

Parameter	Min	Typ	Max	Units
Frequency	22	24	27	MHz

WARNING

Due to XTALOSC automatic level controller, the power consumption depends heavily on the working frequency, C-load and crystal quality. The above results are achieved at a frequency 24 MHz, 10 pF load capacitor, 7 pF crystal shunt capacitor and 80 Ω ESR.

Table 106 shows the XTALOSC_32K electrical specifications.

Table 106. XTALOSC_32K Electrical Specifications

Parameter	Min	Typ	Max	Units
Frequency	--	32.768/32.0[1]	--	kHz

1 Recommended nominal frequency 32.768 kHz.

Table 107 shows the CKIL electrical specifications.

Table 107. CKIL Electrical Specifications

Parameter	Min	Typ	Max	Units
Frequency	16	32.768	50	kHz

4.9 Integrated LDO Voltage Regulators Parameters

The PLL supplies VDD_DIG_PLL and VDD_ANA_PLL can be powered ON from internal LDO voltage regulator (default case). In this case VDD_REG is used as internal regulator's power source. The regulator's output can be used as a supply for other domains such as VDDA and VDDAL1.

Table 108 shows the VDD_DIG_PLL and VDD_ANA_PLL Integrated Voltage Regulators Parameters.

Table 108. LDO Voltage Regulators Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Units
VDD_DIG_PLL functional Voltage Range[1]	$V_{VID_DIG_PLL}$	1.15	1.2	1.3	V
VDD_ANA_PLL functional Voltage Range[1]	$V_{VDD_ANA_PLL}$	1.7	1.8	1.95	V
VDD_DIG_PLL and VDD_ANA_PLL accuracy	—	—	—	+/–3	%
VDD_DIG_PLL power-supply rejection ratio[2]	—	—	–18	—	dB
VDD_ANA_PLL power-supply rejection ratio[2]	—	—	–15	—	dB
Output current[3]	$I_{VID_DIG_PLL}$+ $I_{VDD_ANA_PLL}$	—	—	125	mA

1 VDD_DIG_PLL and VDD_ANA_PLL voltages are programmable, but should not be set outside the target functional range for proper PLL operation.

2 The gain or attenuation from the input supply variation to the output of the LDO (by design).

3 The limitation is for sum of the VDD_DIG_PLL and VDD_ANA_PLL current.

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 109 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see i.MX53 Fuse Map document and System Boot chapter in i.MX53 Reference Manual.

Table 109. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	E-Fuse Name	Details
BOOT_MODE[1]	Input	N/A	Boot Mode selection
BOOT_MODE[0]	Input		

Table 109. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	E-Fuse Name	Details
EIM_A22	Input	BOOT_CFG1[7]/Test Mode Selection	Boot Options, Pin value overrides fuse settings for **BT_FUSE_SEL = '0'**. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
EIM_A21	Input	BOOT_CFG1[6]/Test Mode Selection	
EIM_A20	Input	BOOT_CFG1[5]/Test Mode Selection	
EIM_A19	Input	BOOT_CFG1[4]	
EIM_A18	Input	BOOT_CFG1[3]	
EIM_A17	Input	BOOT_CFG1[2]	
EIM_A16	Input	BOOT_CFG1[1]	
EIM_LBA	Input	BOOT_CFG1[0]	
EIM_EB0	Input	BOOT_CFG2[7]	
EIM_EB1	Input	BOOT_CFG2[6]	
EIM_DA0	Input	BOOT_CFG2[5]	
EIM_DA1	Input	BOOT_CFG2[4]	
EIM_DA2	Input	BOOT_CFG2[3]	
EIM_DA3	Input	BOOT_CFG2[2]	
EIM_DA4	Input	BOOT_CFG3[7]	
EIM_DA5	Input	BOOT_CFG3[6]	
EIM_DA6	Input	BOOT_CFG3[5]	
EIM_DA7	Input	BOOT_CFG3[4]	
EIM_DA8	Input	BOOT_CFG3[3]	
EIM_DA9	Input	BOOT_CFG3[2]	
EIM_DA10	Input	BOOT_CFG3[1]	

5.2 Boot Devices Interfaces Allocation

Table 109 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 110. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	CSPI	EIM_A25, EIM_D21, EIM_D22, EIM_D28	Only SS1 is supported
SPI	ECSPI-1	EIM_D[19:16]	Only SS1 is supported
SPI	ECSPI-2	CSI_DAT[10:8], EIM_LBA	Only SS1 is supported

Table 110. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
EIM	EIM	EIM	• Lower 16 bit data bus A/D multiplexed or upper 16 bit data bus non multiplexed • Only CS0 is supported.
NAND Flash	EXTMC	NAND	• 8/16 bit • NAND data can be muxed either over EIM data or PATA data • Only CS0 is supported
SD/MMC	eSDHCv2-1	PATA_DATA[11:8], SD1_DATA[3:0], SD1_CMD, SD1_CLK	1, 4 or 8 bit
SD/MMC	eSDHCv2-2	PATA_DATA[15:12], SD2_CLK, SD2_CMD, SD2_DATA[3:0]	1, 4 or 8 bit
SD/MMC	eSDHCv3-3	PATA_RESET_B, PATA_IORDY, PATA_DA_0, PATA_DATA[3:0], PATA_DATA[11:8]	1, 4 or 8 bit
SD/MMC	eSDHCv2-4	PATA_DA1, PATA_DA_2, PATA_DATA[7:4], PATA_DATA[15:12]	1, 4 or 8 bit
I2C	I2C-1	EIM_D21, EIM_D28	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D[18:17]	—
PATA	PATA	PATA_DIOW, PATA_DMACK, PATA_DMARQ, PATA_BUFFER_EN, PATA_INTRQ, PATA_DIOR, PATA_RESET_B, PATA_IORDY, PATA_DA_[2:0], PATA_CS_[1:0], PATA_DATA[15:0]	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT, SATA_REFCLKM, SATA_REFCLKP	—
UART	UARTv2-1	CSI0_DAT[11:10]	RXD/TXD only
UART	UARTv2-2	PATA_DMARQ, PATA_BUFFER_EN	RXD/TXD only
UART	UARTv2-3	EIM_D24, EIM_D25	RXD/TXD only
UART	UARTv2-4	CSI0_DAT[13:12]	RXD/TXD only
UART	UARTv2-5	CSI0_DAT[15:14]	RXD/TXD only
USB	USB-OTG PHY	USB_H1_GPANAIO USB_H1_RREFEXT USB_H1_DP USB_H1_DN USB_H1_VBUS	—

5.3 Power setup during Boot

By default, VDD_DIG_PLL is driven from internal on-die 1.2 V linear regulator (LDO). In order to achieve the standard operating mode (see VDD_DIG_PLL on Table 6), LDO output to VDD_DIG_PLL should be configured by software by boot code after power-up to 1.3 V output. This is done by programming the PLL1P2_VREG bits.

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 19x19 mm Package Information

This section contains the outline drawing, signal assignment map, ground/power reference ID (by ball grid location) for the 19 × 19 mm, 0.8 mm pitch package.

6.1.1 Case TEPBGA-2, 19 x 19 mm, 0.8 mm Pitch, 23 x 23 Ball Matrix

Figure 102 shows the top view of the 19×19 mm package, Figure 103 shows the bottom view and the ball location (529 solder balls) of the 19×19 mm package, and Figure 104 shows the side view of the 19×19 mm package.

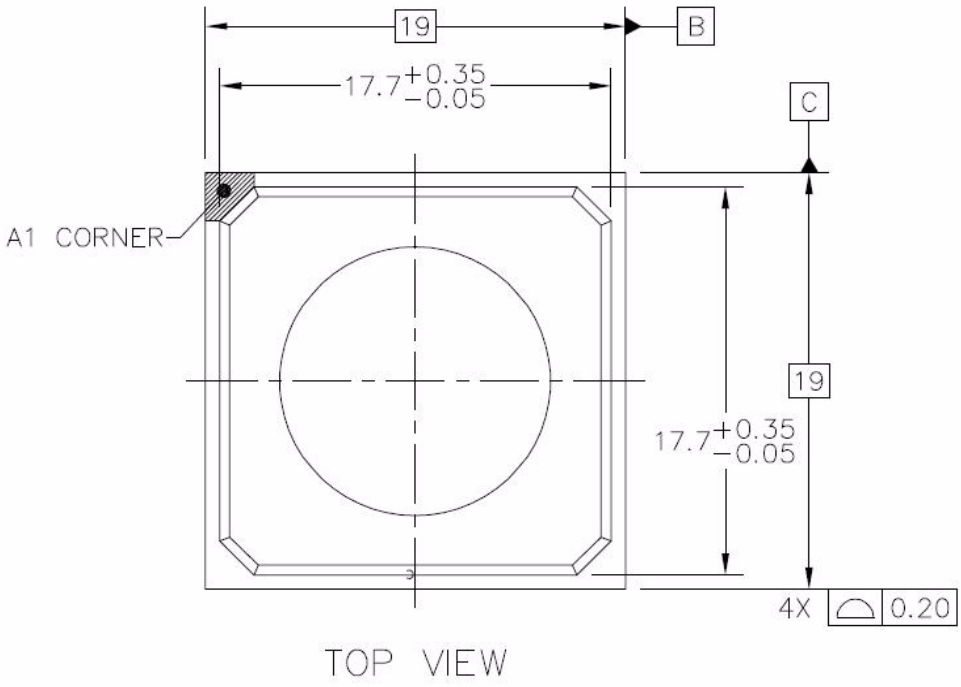


Figure 102. 19 x 19 mm Package Top View

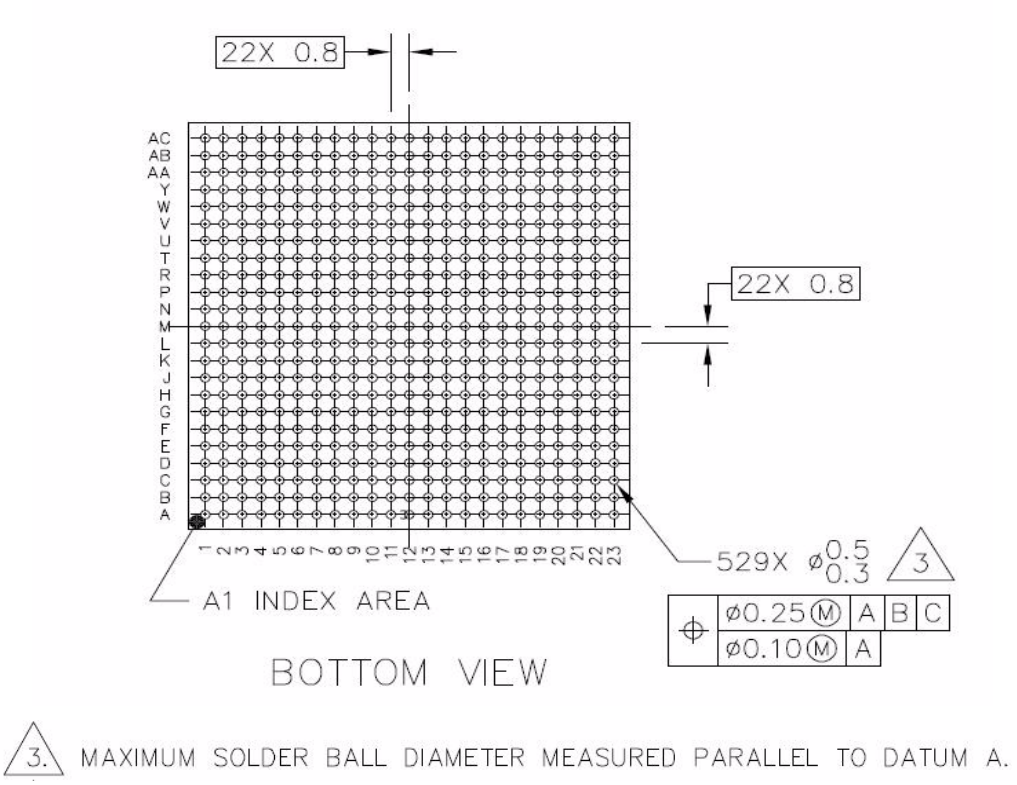


Figure 103. 19 x 19 mm Package, 529 Solder Balls, Bottom View

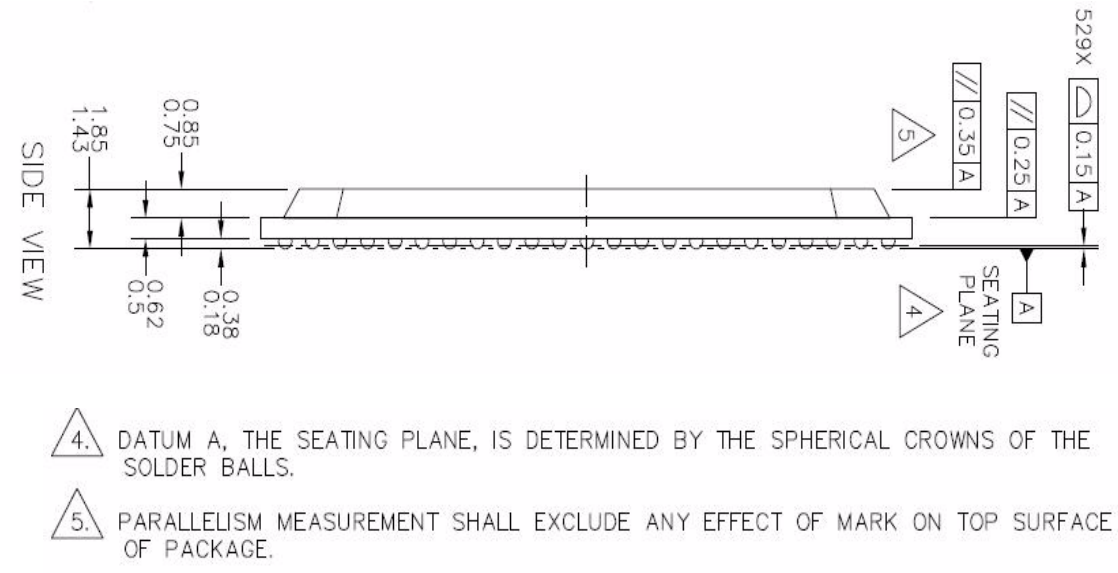


Figure 104. 19 x 19 mm Package Side View

The following notes apply to Figure 102, Figure 103, and Figure 104.

1. All dimensions are in milimeters.
2. Dimensions and tolerencing per ASME Y14.5M1–994.

6.1.2 19 x 19 mm Signal Assignments, Power Rails, and I/O

Table 111 shows the device connection list for ground, power, sense, and reference contact signals.

Table 112 displays an alpha-sorted list of the signal assignments including associated power supplies. The table also includes out of reset pad state. Table 113 shows the package ball map.

6.1.2.1 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

Table 111 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 111. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

Package Pin Name	Package Pin Assignment(s)
DDR_VREF	L17
GND	A1, A11, A13, A18, A2, A22, A23, AA11, AA15, AA20, AA21, AB1, AB18, AB2, AB22, AB23, AC1, AC18, AC2, AC22, AC23, B1, B11, B13, B18, B23, C12, C20, C21, D19, E19, F19, F20, F21, F22, G19, G7, H10, H12, H8, J11, J13, J15, J17, J20, J9, K10, K12, K14, K16, K21, K8, L11, L13, L15, L7, L9, M10, M12, M14, M16, M8, N11, N13, N15, N9, P10, P12, P14, P16, P21, P7, P8, R11, R13, R15, R17, R20, R9, T10, T14, T16, T8, U15, U19, V15, V18, V19, V20, V21, V22, W19, Y14, Y15, Y19
NVCC_CKIH	G17
NVCC_CSI	R7
NVCC_EIM_MAIN	U10, U9
NVCC_EIM_SEC	U7
NVCC_EMI_DRAM	H18, K17, N17, P17, T18
NVCC_FEC	F11
NVCC_GPIO	F8
NVCC_JTAG	G9
NVCC_KEYPAD	F7
NVCC_LCD	J6, J7
NVCC_LVDS	U13
NVCC_LVDS_BG	U14
NVCC_NANDF	T12
NVCC_PATA	N7
NVCC_RESET	H16
NVCC_SD1	H15

Table 111. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

Package Pin Name	Package Pin Assignment(s)
NVCC_SD2	H14
NVCC_SRTC_POW	V11
NVCC_XTAL	V12
SVCC	B22
SVDDGP	B2
TVDAC_AHVDDRGB	U17, V16
TVDAC_DHVDD	U16
USB_H1_VDDA25	F13
USB_H1_VDDA33	G13
USB_OTG_VDDA25	F14
USB_OTG_VDDA33	G14
VCC	H13, J14, J16, K13, K15, L14, L16, M11, M13, M15, M9, N10, N12, N14, N16, N8, P11, P13, P15, P9, R10, R12, R14, R16, R8, T11, T13, T15, T17, T7, T9, U18, U8
VDDA	G12, M17, M7, U12
VDDAL1	F9
VDD_ANA_PLL	G16
VDD_DIG_PLL	H17
VDD_FUSE	G15
VDDGP	G10, G11, G8, H11, H7, H9, J10, J12, J8, K11, K7, K9, L10, L12, L8
VDD_REG	G18
VP	A15, B15
VPH	A9, B9

Table 112 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
BOOT_MODE0	C18	NVCC_RESET	LVIO	ALT0	SRC	src_BOOT_MODE[0]	Input	100 KΩ PD
BOOT_MODE1	B20	NVCC_RESET	LVIO	ALT0	SRC	src_BOOT_MODE[1]	Input	100 KΩ PD
CKIH1	B21	NVCC_CKIH	ANALOG	ALT0	CAMP-1	camp1_CKIH	Input	Analog
CKIH2	D18	NVCC_CKIH	ANALOG	ALT0	CAMP-2	camp2_CKIH	Input	Analog
CKIL	AB10	NVCC_SRTC_POW	ANALOG	—	SRCT	CKIL	—	—
CSI0_DAT10	R5	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[28]	Input	100 KΩ PU
CSI0_DAT11	T2	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[29]	Input	100 KΩ PU
CSI0_DAT12	T3	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[30]	Input	360 KΩ PD
CSI0_DAT13	T6	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[31]	Input	360 KΩ PD
CSI0_DAT14	U1	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[0]	Input	360 KΩ PD
CSI0_DAT15	U2	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[1]	Input	360 KΩ PD
CSI0_DAT16	T4	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[2]	Input	360 KΩ PD
CSI0_DAT17	T5	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[3]	Input	360 KΩ PD
CSI0_DAT18	U3	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[4]	Input	360 KΩ PD
CSI0_DAT19	U4	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[5]	Input	360 KΩ PD
CSI0_DAT4	R1	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[22]	Input	100 KΩ PU
CSI0_DAT5	R2	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[23]	Input	360 KΩ PD
CSI0_DAT6	R6	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[24]	Input	100 KΩ PU
CSI0_DAT7	R3	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[25]	Input	100 KΩ PU
CSI0_DAT8	T1	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[26]	Input	100 KΩ PU
CSI0_DAT9	R4	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[27]	Input	360 KΩ PD
CSI0_DATA_EN	P3	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[20]	Input	100 KΩ PU
CSI0_MCLK	P2	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[19]	Input	100 KΩ PU
CSI0_PIXCLK	P1	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[18]	Input	100 KΩ PU
CSI0_VSYNC	P4	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[21]	Input	100 KΩ PU

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
DI0_DISP_CLK	H4	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[16]	Input	100 KΩ PU
DI0_PIN15	E4	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[17]	Input	100 KΩ PU
DI0_PIN2	D3	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[18]	Input	100 KΩ PU
DI0_PIN3	C2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[19]	Input	100 KΩ PU
DI0_PIN4	D2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[20]	Input	100 KΩ PU
DISP0_DAT0	J5	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[21]	Input	100 KΩ PD
DISP0_DAT1	J4	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[22]	Input	100 KΩ PD
DISP0_DAT10	G3	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[31]	Input	100 KΩ PU
DISP0_DAT11	H5	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[5]	Input	100 KΩ PD
DISP0_DAT12	H1	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[6]	Input	100 KΩ PU
DISP0_DAT13	E1	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[7]	Input	100 KΩ PU
DISP0_DAT14	F2	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[8]	Input	100 KΩ PU
DISP0_DAT15	F3	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[9]	Input	100 KΩ PU
DISP0_DAT16	D1	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[10]	Input	100 KΩ PU
DISP0_DAT17	F5	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[11]	Input	100 KΩ PU
DISP0_DAT18	G4	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[12]	Input	100 KΩ PU
DISP0_DAT19	G5	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[13]	Input	100 KΩ PU
DISP0_DAT2	H2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[23]	Input	100 KΩ PD
DISP0_DAT20	F4	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[14]	Input	100 KΩ PU
DISP0_DAT21	C1	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[15]	Input	100 KΩ PU
DISP0_DAT22	E3	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[16]	Input	100 KΩ PU
DISP0_DAT23	C3	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[17]	Input	100 KΩ PU
DISP0_DAT3	F1	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[24]	Input	100 KΩ PD
DISP0_DAT4	G2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[25]	Input	100 KΩ PD
DISP0_DAT5	H3	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[26]	Input	100 KΩ PD
DISP0_DAT6	G1	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[27]	Input	100 KΩ PD
DISP0_DAT7	H6	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[28]	Input	100 KΩ PD
DISP0_DAT8	G6	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[29]	Input	100 KΩ PU

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
DISP0_DAT9	E2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[30]	Input	100 KΩ PU
DRAM_A0	M19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[0]	Output	Low
DRAM_A1	L21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[1]	Output	Low
DRAM_A10	K19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[10]	Output	Low
DRAM_A11	L22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[11]	Output	Low
DRAM_A12	L20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[12]	Output	Low
DRAM_A13	L23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[13]	Output	Low
DRAM_A14	N18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[14]	Output	Low
DRAM_A15	M18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[15]	Output	Low
DRAM_A2	M20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[2]	Output	Low
DRAM_A3	N20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[3]	Output	Low
DRAM_A4	K20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[4]	Output	Low
DRAM_A5	N21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[5]	Output	Low
DRAM_A6	M22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[6]	Output	Low
DRAM_A7	N22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[7]	Output	Low
DRAM_A8	N23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[8]	Output	Low
DRAM_A9	M21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[9]	Output	Low
DRAM_CALIBRATION	M23	NVCC_EMI_DRAM	special	—	—	(used in DRAM driver calibration. See Special Signal Considerations {add xref} above)	Input	—
DRAM_CAS	L18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CAS	Output	High
DRAM_CS0	K18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CS[0]	Output	High
DRAM_CS1	P19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CS[1]	Output	High

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
DRAM_D0	H20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[0]	Output	High
DRAM_D1	G21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[1]	Output	High
DRAM_D10	E22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[10]	Output	High
DRAM_D11	D20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[11]	Output	High
DRAM_D12	E23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[12]	Output	High
DRAM_D13	C23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[13]	Output	High
DRAM_D14	F23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[14]	Output	High
DRAM_D15	C22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[15]	Output	High
DRAM_D16	U20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[16]	Output	High
DRAM_D17	T21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[17]	Output	High
DRAM_D18	U21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[18]	Output	High
DRAM_D19	R21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[19]	Output	High
DRAM_D2	J21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[2]	Output	High
DRAM_D20	U23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[20]	Output	High
DRAM_D21	R22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[21]	Output	High
DRAM_D22	U22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[22]	Output	High
DRAM_D23	R23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[23]	Output	High
DRAM_D24	Y20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[24]	Output	High
DRAM_D25	W21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[25]	Output	High

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
DRAM_D26	Y21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[26]	Output	High
DRAM_D27	W22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[27]	Output	High
DRAM_D28	AA23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[28]	Output	High
DRAM_D29	V23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[29]	Output	High
DRAM_D3	G20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[3]	Output	High
DRAM_D30	AA22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[30]	Output	High
DRAM_D31	W23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[31]	Output	High
DRAM_D4	J23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[4]	Output	High
DRAM_D5	G23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[5]	Output	High
DRAM_D6	J22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[6]	Output	High
DRAM_D7	G22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[7]	Output	High
DRAM_D8	E21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[8]	Output	High
DRAM_D9	D21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[9]	Output	High
DRAM_DQM0	H21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[0]	Output	Low
DRAM_DQM1	E20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[1]	Output	Low
DRAM_DQM2	T20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[2]	Output	Low
DRAM_DQM3	W20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[3]	Output	Low
DRAM_RAS	J19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_RAS	Output	High
DRAM_RESET	P18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_RESET	Output	Low
DRAM_SDBA0	R19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDBA[0]	Output	Low
DRAM_SDBA1	P20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDBA[1]	Output	Low

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
DRAM_SDBA2	N19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDBA[2]	Output	Low
DRAM_SDCKE0	H19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDCKE[0]	Output	Low
DRAM_SDCKE1	T19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDCKE[1]	Output	Low
DRAM_SDCLK_0	K23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDCLK0	Output	Floating
DRAM_SDCLK_0_B	K22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDCLK0_B	Output	Floating
DRAM_SDCLK_1	P22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDCLK1	Output	Floating
DRAM_SDCLK_1_B	P23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDCLK1_B	Output	Floating
DRAM_SDODT0	J18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_ODT[0]	Output	Low
DRAM_SDODT1	R18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_ODT[1]	Output	Low
DRAM_SDQS0	H23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS[0]	Input	Low
DRAM_SDQS0_B	H22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS_B[0]	Input	High
DRAM_SDQS1	D23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS[1]	Input	Low
DRAM_SDQS1_B	D22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS_B[1]	Input	High
DRAM_SDQS2	T22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS[2]	Input	Low
DRAM_SDQS2_B	T23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS_B[2]	Input	High
DRAM_SDQS3	Y22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS[3]	Input	Low
DRAM_SDQS3_B	Y23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS_B[3]	Input	High
DRAM_SDWE	L19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDWE	Output	High

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
ECKIL	AC10	NVCC_SRTC_POW	ANALOG	—	SRTC	ECKIL {no block I/O by this name in RM}	—	—
EIM_A16	AA5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[16]	Output[2]	—
EIM_A17	V7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[17]	Output[2]	—
EIM_A18	AB3	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[18]	Output[2]	—
EIM_A19	W7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[19]	Output[2]	—
EIM_A20	Y6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[20]	Output[2]	—
EIM_A21	AA4	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[21]	Output[2]	—
EIM_A22	AA3	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[22]	Output[2]	—
EIM_A23	V6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[23]	Output	—
EIM_A24	Y5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[24]	Output	—
EIM_A25	W6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[25]	Output	—
EIM_BCLK	W11	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_BCLK	Output	—
EIM_CS0	W8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_CS[0]	Output	—
EIM_CS1	Y7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_CS[1]	Output	—
EIM_D16	U6	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[16]	Input	100 KΩ PU
EIM_D17	U5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[17]	Input	100 KΩ PU
EIM_D18	V1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[18]	Input	100 KΩ PU
EIM_D19	V2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[19]	Input	100 KΩ PU
EIM_D20	W1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[20]	Input	100 KΩ PU
EIM_D21	V3	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[21]	Input	100 KΩ PU
EIM_D22	W2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[22]	Input	360 KΩ PD
EIM_D23	Y1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[23]	Input	100 KΩ PU
EIM_D24	Y2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[24]	Input	100 KΩ PU
EIM_D25	W3	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[25]	Input	100 KΩ PU
EIM_D26	V5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[26]	Input	100 KΩ PU
EIM_D27	V4	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[27]	Input	100 KΩ PU
EIM_D28	AA1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[28]	Input	100 KΩ PU
EIM_D29	AA2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[29]	Input	100 KΩ PU

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
EIM_D30	W4	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[30]	Input	100 KΩ PU
EIM_D31	W5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[31]	Input	360 KΩ PD
EIM_DA0	Y8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[0]	Input[2]	100 KΩ PU
EIM_DA1	AC4	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[1]	Input[2]	100 KΩ PU
EIM_DA10	AB7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[10]	Input[2]	100 KΩ PU
EIM_DA11	AC6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[11]	Input	100 KΩ PU
EIM_DA12	V10	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[12]	Input	100 KΩ PU
EIM_DA13	AC7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[13]	Input	100 KΩ PU
EIM_DA14	Y10	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[14]	Input	100 KΩ PU
EIM_DA15	AA9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[15]	Input	100 KΩ PU
EIM_DA2	AA7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[2]	Input[2]	100 KΩ PU
EIM_DA3	W9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[3]	Input[2]	100 KΩ PU
EIM_DA4	AB6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[4]	Input[2]	100 KΩ PU
EIM_DA5	V9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[5]	Input[2]	100 KΩ PU
EIM_DA6	Y9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[6]	Input[2]	100 KΩ PU
EIM_DA7	AC5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[7]	Input[2]	100 KΩ PU
EIM_DA8	AA8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[8]	Input[2]	100 KΩ PU
EIM_DA9	W10	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[9]	Input[2]	100 KΩ PU
EIM_EB0	AC3	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_EB[0]	Output[2]	—

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
EIM_EB1	AB5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_EB[1]	Output[2]	—
EIM_EB2	Y3	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-2	gpio2_GPIO[30]	Input	100 KΩ PU
EIM_EB3	Y4	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-2	gpio2_GPIO[31]	Input	100 KΩ PU
EIM_LBA	AA6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_LBA	Output[2]	—
EIM_OE	V8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_OE	Output	—
EIM_RW	AB4	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_RW	Output	—
EIM_WAIT	AB9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_WAIT	Output	—
EXTAL	AB11	NVCC_XTAL	ANALOG	—	EXTAL OSC	EXTAL	—	—
FASTR_ANA	E18	NVCC_CKIH	ANALOG	—	—	(reserved, tie to ground)	—	—
FASTR_DIG	E17	NVCC_CKIH	ANALOG	—	—	(reserved, tie to ground)	—	—
FEC_CRS_DV	D11	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[25]	Input	100 KΩ PU
FEC_MDC	E10	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[31]	Input	100 KΩ PU
FEC_MDIO	D12	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[22]	Input	100 KΩ PU
FEC_REF_CLK	E12	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[23]	Input	100 KΩ PU
FEC_RX_ER	F12	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[24]	Input	100 KΩ PU
FEC_RXD0	C11	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[27]	Input	100 KΩ PU
FEC_RXD1	E11	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[26]	Input	100 KΩ PU
FEC_TX_EN	C10	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[28]	Input	360 KΩ PD
FEC_TXD0	F10	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[30]	Input	100 KΩ PU
FEC_TXD1	D10	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[29]	Input	100 KΩ PU
GPIO_0	C8	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[0]	Input	360 KΩ PD
GPIO_1	B7	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[1]	Input	360 KΩ PD
GPIO_10	W16	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[0]	Input	100 KΩ PU
GPIO_11	V17	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[1]	Input	100 KΩ PU
GPIO_12	W17	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[2]	Input	100 KΩ PU

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
GPIO_13	AA18	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[3]	Input	100 KΩ PU
GPIO_14	W18	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[4]	Input	100 KΩ PU
GPIO_16	C6	NVCC_GPIO	UHVIO	ALT1	GPIO-7	gpio7_GPIO[11]	Input	360 KΩ PD
GPIO_17	A3	NVCC_GPIO	UHVIO	ALT1	GPIO-7	gpio7_GPIO[12]	Input	360 KΩ PD
GPIO_18	D7	NVCC_GPIO	UHVIO	ALT1	GPIO-7	gpio7_GPIO[13]	Input	360 KΩ PD
GPIO_19	B4	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[5]	Input[3]	100 KΩ PU
GPIO_2	C7	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[2]	Input	360 KΩ PD
GPIO_3	A6	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[3]	Input	360 KΩ PD
GPIO_4	D8	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[4]	Input	100 KΩ PU
GPIO_5	A5	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[5]	Input	360 KΩ PD
GPIO_6	B6	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[6]	Input	360 KΩ PD
GPIO_7	A4	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[7]	Input	360 KΩ PD
GPIO_8	B5	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[8]	Input	360 KΩ PD
GPIO_9	E8	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[9]	Input	100 KΩ PU
JTAG_MOD	C9	NVCC_JTAG	GPIO	ALT0	SJC	sjc_MOD	Input	100 KΩ PU
JTAG_TCK	D9	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TCK	Input	100 KΩ PD
JTAG_TDI	B8	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TDI	Input	47 KΩ PU
JTAG_TDO	A7	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TDO	Input	Keeper
JTAG_TMS	A8	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TMS	Input	47 KΩ PU
JTAG_TRSTB	E9	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TRSTB	Input	47 KΩ PU
KEY_COL0	C5	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[6]	Input[4]	100 KΩ PU
KEY_COL1	E7	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[8]	Input	100 KΩ PU
KEY_COL2	C4	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[10]	Input	100 KΩ PU
KEY_COL3	F6	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[12]	Input	100 KΩ PU
KEY_COL4	E5	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[14]	Input	100 KΩ PU
KEY_ROW0	B3	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[7]	Input	360 KΩ PD
KEY_ROW1	D6	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[9]	Input	100 KΩ PU
KEY_ROW2	D5	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[11]	Input	100 KΩ PU

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
KEY_ROW3	D4	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[13]	Input	100 KΩ PU
KEY_ROW4	E6	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[15]	Input	360 KΩ PD
LVDS_BG_RES	AA14	NVCC_LVDS_BG	ANALOG	—	LDB	LVDS_BG_RES	—	—
LVDS0_CLK_N	AB16	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[25]	Input	Floating
LVDS0_CLK_P	AC16	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[24]	Input	Floating
LVDS0_TX0_N	Y17	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[31]	Input	Floating
LVDS0_TX0_P	AA17	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[30]	Input	Floating
LVDS0_TX1_N	AB17	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[29]	Input	Floating
LVDS0_TX1_P	AC17	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[28]	Input	Floating
LVDS0_TX2_N	Y16	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[27]	Input	Floating
LVDS0_TX2_P	AA16	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[26]	Input	Floating
LVDS0_TX3_N	AB15	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[23]	Input	Floating
LVDS0_TX3_P	AC15	NVCC_LVDS	LVDS	ALT0	GPIO-7	gpio7_GPI[22]	Input	Floating
LVDS1_CLK_N	AA13	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[27]	Input	Floating
LVDS1_CLK_P	Y13	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[26]	Input	Floating
LVDS1_TX0_N	AC14	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[31]	Input	Floating
LVDS1_TX0_P	AB14	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[30]	Input	Floating
LVDS1_TX1_N	AC13	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[29]	Input	Floating
LVDS1_TX1_P	AB13	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[28]	Input	Floating
LVDS1_TX2_N	AC12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[25]	Input	Floating
LVDS1_TX2_P	AB12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[24]	Input	Floating

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
LVDS1_TX3_N	AA12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[23]	Input	Floating
LVDS1_TX3_P	Y12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[22]	Input	Floating
NANDF_ALE	Y11	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[8]	Input	100 KΩ PU
NANDF_CLE	AA10	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[7]	Input	100 KΩ PU
NANDF_CS0	W12	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[11]	Input	100 KΩ PU
NANDF_CS1	V13	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[14]	Input	100 KΩ PU
NANDF_CS2	V14	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[15]	Input	100 KΩ PU
NANDF_CS3	W13	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[16]	Input	100 KΩ PU
NANDF_RB0	U11	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[10]	Input	100 KΩ PU
NANDF_RE_B	AC8	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-6	gpio6_GPIO[13]	Input	100 KΩ PU
NANDF_WE_B	AB8	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-6	gpio6_GPIO[12]	Input	100 KΩ PU
NANDF_WP_B	AC9	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[9]	Input	100 KΩ PU
PATA_BUFFER_EN	K4	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[1]	Input	100 KΩ PU
PATA_CS_0	L5	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[9]	Input	100 KΩ PU
PATA_CS_1	L2	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[10]	Input	100 KΩ PU
PATA_DA_0	K6	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[6]	Input	100 KΩ PU
PATA_DA_1	L3	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[7]	Input	100 KΩ PU
PATA_DA_2	L4	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[8]	Input	100 KΩ PU
PATA_DATA0	L1	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[0]	Input	100 KΩ PU
PATA_DATA1	M1	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[1]	Input	100 KΩ PU
PATA_DATA10	N4	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[10]	Input	100 KΩ PU
PATA_DATA11	M6	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[11]	Input	100 KΩ PU
PATA_DATA12	N5	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[12]	Input	100 KΩ PU
PATA_DATA13	N6	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[13]	Input	100 KΩ PU
PATA_DATA14	P6	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[14]	Input	100 KΩ PU
PATA_DATA15	P5	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[15]	Input	100 KΩ PU

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
PATA_DATA2	L6	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[2]	Input	100 KΩ PU
PATA_DATA3	M2	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[3]	Input	100 KΩ PU
PATA_DATA4	M3	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[4]	Input	100 KΩ PU
PATA_DATA5	M4	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[5]	Input	100 KΩ PU
PATA_DATA6	N1	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[6]	Input	100 KΩ PU
PATA_DATA7	M5	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[7]	Input	100 KΩ PU
PATA_DATA8	N2	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[8]	Input	100 KΩ PU
PATA_DATA9	N3	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[9]	Input	100 KΩ PU
PATA_DIOR	K3	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[3]	Input	100 KΩ PU
PATA_DIOW	J3	NVCC_PATA	UHVIO	ALT1	GPIO-6	gpio6_GPIO[17]	Input	100 KΩ PU
PATA_DMACK	J2	NVCC_PATA	UHVIO	ALT1	GPIO-6	gpio6_GPIO[18]	Input	100 KΩ PU
PATA_DMARQ	J1	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[0]	Input	100 KΩ PU
PATA_INTRQ	K5	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[2]	Input	100 KΩ PU
PATA_IORDY	K1	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[5]	Input	100 KΩ PU
PATA_RESET_B	K2	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[4]	Input	100 KΩ PU
PMIC_ON_REQ	W14	NVCC_SRTC_POW	GPIO	ALT0	SRTC	srtc_SRTCALARM	Output	—
PMIC_STBY_REQ	W15	NVCC_SRTC_POW	GPIO	ALT0	CCM	ccm_PMIC_VSTBY_REQ	Output	—
POR_B	C19	NVCC_RESET	LVIO	ALT0	SRC	src_POR_B	Input	100 KΩ PU
RESET_IN_B	A21	NVCC_RESET	LVIO	ALT0	SRC	src_RESET_B	Input	100 KΩ PU
SATA_REFCLKM	A14	VPH	ANALOG	—	SATA	SATA_REFCLKM	—	—
SATA_REFCLKP	B14	VPH	ANALOG	—	SATA	SATA_REFCLKP	—	—
SATA_REXT	C13	VPH	ANALOG	—	SATA	SATA_REXT	—	—
SATA_RXM	A12	VPH	ANALOG	—	SATA	SATA_RXM	—	—
SATA_RXP	B12	VPH	ANALOG	—	SATA	SATA_RXP	—	—
SATA_TXM	B10	VPH	ANALOG	—	SATA	SATA_TXM	—	—
SATA_TXP	A10	VPH	ANALOG	—	SATA	SATA_TXP	—	—

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
SD1_CLK	E16	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[20]	Input	100 KΩ PU
SD1_CMD	F18	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[18]	Input	100 KΩ PU
SD1_DATA0	A20	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[16]	Input	100 KΩ PU
SD1_DATA1	C17	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[17]	Input	100 KΩ PU
SD1_DATA2	F17	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[19]	Input	100 KΩ PU
SD1_DATA3	F16	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[21]	Input	100 KΩ PU
SD2_CLK	E14	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[10]	Input	100 KΩ PU
SD2_CMD	C15	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[11]	Input	100 KΩ PU
SD2_DATA0	D13	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[15]	Input	100 KΩ PU
SD2_DATA1	C14	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[14]	Input	100 KΩ PU
SD2_DATA2	D14	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[13]	Input	100 KΩ PU
SD2_DATA3	E13	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[12]	Input	100 KΩ PU
TEST_MODE	D17	NVCC_RESET	LVIO	ALT0		tcu_TEST_MODE	Input	100 KΩ PD
TVCDC_IOB_BACK	AB19	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVCDC_IOB_BACK	—	—
TVCDC_IOG_BACK	AC20	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVCDC_IOG_BACK	—	—
TVCDC_IOR_BACK	AB21	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVCDC_IOR_BACK	—	—
TVDAC_COMP	AA19	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_COMP	—	—
TVDAC_IOB	AC19	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_IOB	—	—
TVDAC_IOG	AB20	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_IOG	—	—
TVDAC_IOR	AC21	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_IOR	—	—
TVDAC_VREF	Y18	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_VREF	—	—
USB_H1_DN	B17	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB	USB_H1_DN	—	—

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
USB_H1_DP	A17	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB	USB_H1_DP	—	—
USB_H1_GPANAIO	A16	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	USB	USB_H1_GPANAIO	—	—
USB_H1_RREFEXT	B16	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	USB	USB_H1_RREFEXT	—	—
USB_H1_VBUS	D15	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB	USB_H1_VBUS	—	—
USB_OTG_DN	A19	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB	USB_OTG_DN	—	—
USB_OTG_DP	B19	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB	USB_OTG_DP	—	—
USB_OTG_GPANAIO	F15	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB	USB_OTG_GPANAIO	—	—
USB_OTG_ID	C16	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB	USB_OTG_ID	—	—
USB_OTG_RREFEXT	D16	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB	USB_OTG_RREFEXT	—	—
USB_OTG_VBUS	E15	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB	USB_OTG_VBUS	—	—
XTAL	AC11	NVCC_XTAL	ANALOG	—	XTALOSC	XTAL	—	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 During power-on reset this port acts as input for fuse override, ~33KΩ PU/PD recommended to set the value. See Section 5.1, “Boot Mode Configuration Pins” for details.

3 During power-on reset this port acts as output for diagnostic signal INT_BOOT

4 During power-on reset this port acts as output for diagnostic signal ANY_PU_RST

NOTE

KEY_COL0 and GPIO_19 act as output for diagnostic signals during power-on reset.

6.2 19 x 19 mm, 0.8 Pitch Ball Map

Table 113 shows the 19 × 19 mm, 0.8 pitch ball map.

Table 113. 19 × 19 mm, 0.8 Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	GND	GPIO_17	GPIO_7	GPIO_5	GPIO_3	JTAG_TDO	JTAG_TMS	VPH	SATA_TXP	GND	SATA_RXM	GND	SATA_REFCLKM	VP	USB_H1_GPANAIO	USB_H1_DP	GND	USB_OTG_DN	SD1_DATA0	RESET_IN_B	GND	GND	A
B	GND	SVDDGP	KEY_ROW0	GPIO_19	GPIO_8	GPIO_6	GPIO_1	JTAG_TDI	VPH	SATA_TXM	GND	SATA_RXP	GND	SATA_REFCLKP	VP	USB_H1_RREFEXT	USB_H1_DN	GND	USB_OTG_DP	BOOT_MODE1	CKIH1	SVCC	GND	B
C	DISP0_DAT21	DI0_PIN3	DISP0_DAT23	KEY_COL2	KEY_COL0	GPIO_16	GPIO_2	GPIO_0	JTAG_MOD	FEC_TX_EN	FEC_RXD0	GND	SATA_REXT	SD2_DATA1	SD2_CMD	USB_OTG_ID	SD1_DATA1	BOOT_MODE0	POR_B	GND	GND	DRAM_D15	DRAM_D13	C
D	DISP0_DAT16	DI0_PIN4	DI0_PIN2	KEY_ROW3	KEY_ROW2	KEY_ROW1	GPIO_18	GPIO_4	JTAG_TCK	FEC_TXD1	FEC_CRS_DV	FEC_MDIO	SD2_DATA0	SD2_DATA2	USB_H1_VBUS	USB_OTG_RREFEXT	TEST_MODE	CKIH2	GND	DRAM_D11	DRAM_D9	DRAM_SDQS1_B	DRAM_SDQS1	D
E	DISP0_DAT13	DISP0_DAT9	DISP0_DAT22	DI0_PIN15	KEY_COL4	KEY_ROW4	KEY_COL1	GPIO_9	JTAG_TRSTB	FEC_MDC	FEC_RXD1	FEC_REF_CLK	SD2_DATA3	SD2_CLK	USB_OTG_VBUS	SD1_CLK	FASTR_DIG	FASTR_ANA	GND	DRAM_DQM1	DRAM_D8	DRAM_D10	DRAM_D12	E
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Table 113. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	L	K	J	H	G	F	
1	PATA_DATA0	PATA_IORDY	PATA_DMARQ	DISP0_DAT12	DISP0_DAT6	DISP0_DAT3	1
2	PATA_CS_1	PATA_RESET_B	PATA_DMACK	DISP0_DAT2	DISP0_DAT4	DISP0_DAT14	2
3	PATA_DA_1	PATA_DIOR	PATA_DIOW	DISP0_DAT5	DISP0_DAT10	DISP0_DAT15	3
4	PATA_DA_2	PATA_BUFFER_EN	DISP0_DAT1	DI0_DISP_CLK	DISP0_DAT18	DISP0_DAT20	4
5	PATA_CS_0	PATA_INTRQ	DISP0_DAT0	DISP0_DAT11	DISP0_DAT19	DISP0_DAT17	5
6	PATA_DATA2	PATA_DA_0	NVCC_LCD	DISP0_DAT7	DISP0_DAT8	KEY_COL3	6
7	GND	VDDGP	NVCC_LCD	VDDGP	GND	NVCC_KEYPAD	7
8	VDDGP	GND	VDDGP	GND	VDDGP	NVCC_GPIO	8
9	GND	VDDGP	GND	VDDGP	NVCC_JTAG	VDDAL1	9
10	VDDGP	GND	VDDGP	GND	VDDGP	FEC_TXD0	10
11	GND	VDDGP	GND	VDDGP	VDDGP	NVCC_FEC	11
12	VDDGP	GND	VDDGP	GND	VDDA	FEC_RX_ER	12
13	GND	VCC	GND	VCC	USB_H1_VDDA33	USB_H1_VDDA25	13
14	VCC	GND	VCC	NVCC_SD2	USB_OTG_VDDA33	USB_OTG_VDDA25	14
15	GND	VCC	GND	NVCC_SD1	VDD_FUSE	USB_OTG_GPANAIO	15
16	VCC	GND	VCC	NVCC_RESET	VDD_ANA_PLL	SD1_DATA3	16
17	DDR_VREF	NVCC_EMI_DRAM	GND	VDD_DIG_PLL	NVCC_CKIH	SD1_DATA2	17
18	DRAM_CAS	DRAM_CS0	DRAM_SDODT0	NVCC_EMI_DRAM	VDD_REG	SD1_CMD	18
19	DRAM_SDWE	DRAM_A10	DRAM_RAS	DRAM_SDCKE0	GND	GND	19
20	DRAM_A12	DRAM_A4	GND	DRAM_D0	DRAM_D3	GND	20
21	DRAM_A1	GND	DRAM_D2	DRAM_DQM0	DRAM_D1	GND	21
22	DRAM_A11	DRAM_SDCLK_0_B	DRAM_D6	DRAM_SDQS0_B	DRAM_D7	GND	22
23	DRAM_A13	DRAM_SDCLK_0	DRAM_D4	DRAM_SDQS0	DRAM_D5	DRAM_D14	23
	L	K	J	H	G	F	

Table 113. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	U	T	R	P	N	M	
1	CSI0_DAT14	CSI0_DAT8	CSI0_DAT4	CSI0_PIXCLK	PATA_DATA6	PATA_DATA1	1
2	CSI0_DAT15	CSI0_DAT11	CSI0_DAT5	CSI0_MCLK	PATA_DATA8	PATA_DATA3	2
3	CSI0_DAT18	CSI0_DAT12	CSI0_DAT7	CSI0_DATA_EN	PATA_DATA9	PATA_DATA4	3
4	CSI0_DAT19	CSI0_DAT16	CSI0_DAT9	CSI0_VSYNC	PATA_DATA10	PATA_DATA5	4
5	EIM_D17	CSI0_DAT17	CSI0_DAT10	PATA_DATA15	PATA_DATA12	PATA_DATA7	5
6	EIM_D16	CSI0_DAT13	CSI0_DAT6	PATA_DATA14	PATA_DATA13	PATA_DATA11	6
7	NVCC_EIM_SEC	VCC	NVCC_CSI	GND	NVCC_PATA	VDDA	7
8	VCC	GND	VCC	GND	VCC	GND	8
9	NVCC_EIM_MAIN	VCC	GND	VCC	GND	VCC	9
10	NVCC_EIM_MAIN	GND	VCC	GND	VCC	GND	10
11	NANDF_RB0	VCC	GND	VCC	GND	VCC	11
12	VDDA	NVCC_NANDF	VCC	GND	VCC	GND	12
13	NVCC_LVDS	VCC	GND	VCC	GND	VCC	13
14	NVCC_LVDS_BG	GND	VCC	GND	VCC	GND	14
15	GND	VCC	GND	VCC	GND	VCC	15
16	TVDAC_DHVDD	GND	VCC	GND	VCC	GND	16
17	TVDAC_AHVDDRGB	VCC	GND	NVCC_EMI_DRAM	NVCC_EMI_DRAM	VDDA	17
18	VCC	NVCC_EMI_DRAM	DRAM_SDODT1	DRAM_RESET	DRAM_A14	DRAM_A15	18
19	GND	DRAM_SDCKE1	DRAM_SDBA0	DRAM_CS1	DRAM_SDBA2	DRAM_A0	19
20	DRAM_D16	DRAM_DQM2	GND	DRAM_SDBA1	DRAM_A3	DRAM_A2	20
21	DRAM_D18	DRAM_D17	DRAM_D19	GND	DRAM_A5	DRAM_A9	21
22	DRAM_D22	DRAM_SDQS2	DRAM_D21	DRAM_SDCLK_1	DRAM_A7	DRAM_A6	22
23	DRAM_D20	DRAM_SDQS2_B	DRAM_D23	DRAM_SDCLK_1_B	DRAM_A8	DRAM_CALIBRATION	23
	U	T	R	P	N	M	

Table 113. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	AC	AB	AA	Y	W	V	
1	GND	GND	EIM_D28	EIM_D23	EIM_D20	EIM_D18	1
2	GND	GND	EIM_D29	EIM_D24	EIM_D22	EIM_D19	2
3	EIM_EB0	EIM_A18	EIM_A22	EIM_EB2	EIM_D25	EIM_D21	3
4	EIM_DA1	EIM_RW	EIM_A21	EIM_EB3	EIM_D30	EIM_D27	4
5	EIM_DA7	EIM_EB1	EIM_A16	EIM_A24	EIM_D31	EIM_D26	5
6	EIM_DA11	EIM_DA4	EIM_LBA	EIM_A20	EIM_A25	EIM_A23	6
7	EIM_DA13	EIM_DA10	EIM_DA2	EIM_CS1	EIM_A19	EIM_A17	7
8	NANDF_RE_B	NANDF_WE_B	EIM_DA8	EIM_DA0	EIM_CS0	EIM_OE	8
9	NANDF_WP_B	EIM_WAIT	EIM_DA15	EIM_DA6	EIM_DA3	EIM_DA5	9
10	ECKIL	CKIL	NANDF_CLE	EIM_DA14	EIM_DA9	EIM_DA12	10
11	XTAL	EXTAL	GND	NANDF_ALE	EIM_BCLK	NVCC_SRTC_POW	11
12	LVDS1_TX2_N	LVDS1_TX2_P	LVDS1_TX3_N	LVDS1_TX3_P	NANDF_CS0	NVCC_XTAL	12
13	LVDS1_TX1_N	LVDS1_TX1_P	LVDS1_CLK_N	LVDS1_CLK_P	NANDF_CS3	NANDF_CS1	13
14	LVDS1_TX0_N	LVDS1_TX0_P	LVDS_BG_RES	GND	PMIC_ON_REQ	NANDF_CS2	14
15	LVDS0_TX3_P	LVDS0_TX3_N	GND	GND	PMIC_STBY_REQ	GND	15
16	LVDS0_CLK_P	LVDS0_CLK_N	LVDS0_TX2_P	LVDS0_TX2_N	GPIO_10	TVDAC_AHVDDRGB	16
17	LVDS0_TX1_P	LVDS0_TX1_N	LVDS0_TX0_P	LVDS0_TX0_N	GPIO_12	GPIO_11	17
18	GND	GND	GPIO_13	TVDAC_VREF	GPIO_14	GND	18
19	TVDAC_IOB	TVCDC_IOB_BACK	TVDAC_COMP	GND	GND	GND	19
20	TVCDC_IOG_BACK	TVDAC_IOG	GND	DRAM_D24	DRAM_DQM3	GND	20
21	TVDAC_IOR	TVCDC_IOR_BACK	GND	DRAM_D26	DRAM_D25	GND	21
22	GND	GND	DRAM_D30	DRAM_SDQS3	DRAM_D27	GND	22
23	GND	GND	DRAM_D28	DRAM_SDQS3_B	DRAM_D31	DRAM_D29	23
	AC	AB	AA	Y	W	V	

7 Revision History

Table 114 provides a revision history for this data sheet.

Table 114. i.MX53xA Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)

Rev 1	3/2011	• Updated the first sentence of Section 3.1, “Special Signal Considerations.”
		• Deleted two tables, “Special Signal Considerations” and “JTAG Controller Interface Summary,” in Section 3.1, “Special Signal Considerations.”
		• Updated Table 6, "i.MX53xA Operating Ranges," on page 19.
		  • Changed VDDGP voltages as follows:
		  — 800 MHz from 1.0/1.05/1.1 to 1.05/1.1/1.15 V minimum/nominal/maximum.
		  — Stop mode from 0.9/0.95/1.1 to 0.8/0.85/1.15 V minimum/nominal/maximum.
		  • Added statements to footnotes 4 and 5.

Rev 0	02/2011	Initial release.

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